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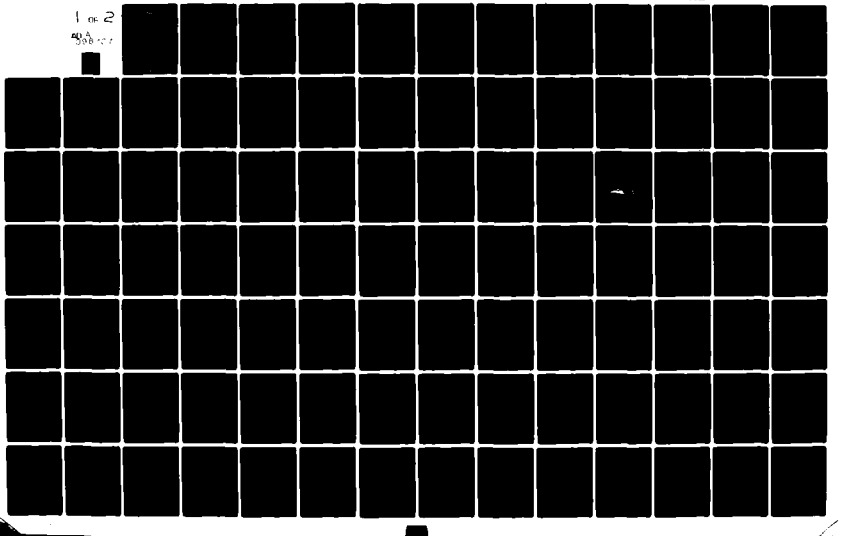

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NUCLEAR EFFECTS TEST PROGRAM FOR THE DSCS III COMMUNICATION SYSTEM

A. R. Harcar
General Electric Company
Space Division
P.O. Box 8555
Philadelphia, Pennsylvania 19101

21 July 1980

Final Report for Period 1 April 1975—1 February 1980

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20 ABSTRACT (Continue on reverse side if necessary and identify by block number)

We have examined the feasibility of testing the DSCS III communication system in a simulated nuclear propagation environment. A set of simulation hardware and software requirements have been derived on the basis of a channel scattering function characterization supplied by the Defense Nuclear Agency and the use of classical statistical communications theory.

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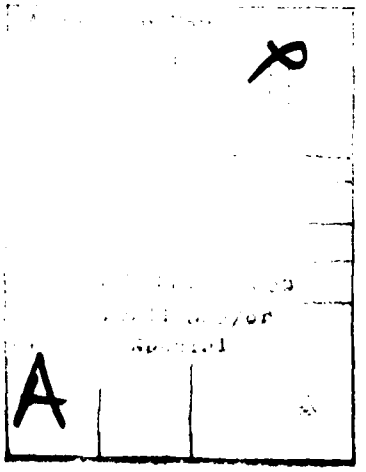
20. ABSTRACT (Continued)

We show that the channel statistics can be reproduced by a time-varying linear filter implemented with a tapped delay line having complex weights chosen from independent Gaussian distributions of appropriate variance.

Test methods and schedules, hardware descriptions, software requirements and a hardware design plan are described. Cost factors have been provided under separate cover.

PREFACE

We would like to express our appreciation for the efforts of Clark Hafer who developed the simulation requirements and the algorithms for the generation of the delay line tap weights. James Blike performed the processor architectural tradeoffs and the digital and firmware design. Don Keer and Clark Hafer developed the off-line software requirements while Herman Jankowski performed trades and developed requirements for R.F./I.F. components.



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SECTION 1
INTRODUCTION

The detonation of a nuclear device at high altitude results in modifications to the ionization density and structure of the earth's ionosphere. This phenomenon affects earth-satellite communication links; propagation of radio waves through this disturbed medium results in the production of amplitude and phase perturbations of the wavefront. In the general case, the phenomenological result is a scintillating, fading signal at the receiver.

The principal objective of this eight-months study has been to establish the feasibility of testing selected portions of the DSCS III satellite system in a simulated nuclear propagation environment. Fading characteristics of these channels are described by means of a channel scattering function.

The Defense Nuclear Agency has furnished the General Electric Company with the scattering function equation and the necessary worst case ranges for each of the variables at X-Band (nominal 8 GHz) frequencies. Evaluation of the scattering function has been completed and the results have been used to derive the requirements for a fading simulator that is capable of reproducing the scintillation experienced by a signal which is passing through a disturbed ionosphere.

Simulator implementation will be in the form of a processor-controlled time-varying linear filter. Filter tap weights will be varied in accordance with the outcome of analog and digital signal processing techniques which emulate the phenomenological effects of the disturbed ionosphere. The output signal statistics of the simulator will have a Rayleigh amplitude distribution and a uniform phase distribution.

SECTION 2
SUMMARY

The principal results of this study have been the derivation of requirements for a fading simulator that produces scintillation type fading and its conceptual design. Design requirements have been derived on the basis of channel models furnished by the Defense Nuclear Agency and conventional statistical communications theory.

The trend towards the increased rise of digital modulation has led to the selection of Bit Error Rate as a test criteria for determination of communications performance in the presence of fading. Command and Telemetry subsystem performance determination is more complex, relying upon a combination of Bit Error Rate, Command Reject, Command Accept and Loss of Lock indications, as noted in Section 3.

Hardware assets needed to perform such tests have been defined. One item, the fading simulator, has been designated as an item to be constructed.

General Electric has designed algorithms for implementing the fading process. Control over the fading simulation will be accomplished through the off-line generation of the tap weights of a densely-tapped delay line. The delay-line and the tap weight modules constitute a time-varying linear filter.

In Section 4, we show that the channel statistics can be reproduced by this time-varying linear filter implemented with a tapped delay line having complex weights chosen from independent Gaussian distributions having appropriate variance. The process used to generate the complex weights can occur independently and off-line from the experimental determination of the effects upon the communications signal, as is shown in Figure 1.

The complex weights modulate the in-phase and quadrature components of the signal. The linear summation of the time-delayed outputs of these two independent Gaussian processes results in a signal having Rayleigh amplitude statistics with uniformly distributed phase. In the case of uplink signal modifications, the random modulation process will occur prior to reception by the satellite. Since the satellite payload has different performance characteristics in the linear and in the non-linear modes, both uplink and downlink signal modifications must be considered. Conventional error detection and analysis will then follow.

Test procedures for the DSCS III SHF communications subsystem emphasize TDMA performance characteristics. Therefore, the simulation hardware is designed to accomodate the maximum bandwidths of the satellite channels and still produce negligible distortion. Maximum channel bandwidths are stated in Table 1 and the simulator bandwidth is nominally set at 100 MHz to provide a margin.

SIMULATION CONCEPT

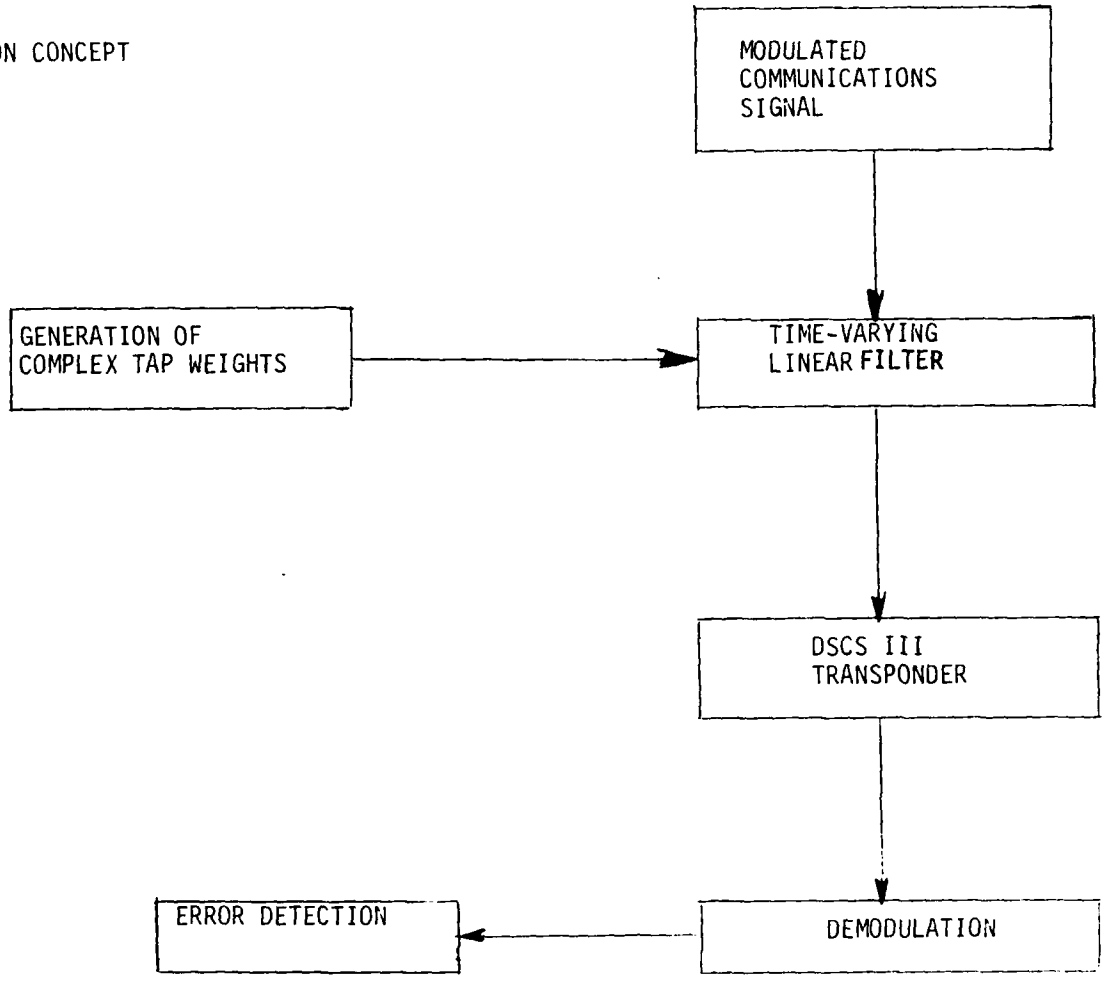

Figure 1. Simulation concept.

Table 1. Maximum data rates and channel bandwidths.

CHANNEL	DESIGNATED BANDWIDTH	EFFECTED NOISE BANDWIDTH (NOMINAL)	BIT RATE (MEGABITS/SECOND)
1, 2, 4, 5	60 MHz	72 MHz	80*
3	85	102	113*
6	50	60	67*
SHF COMMAND	BATSON I, II	BATSON I, II	BATSON I, II
* BASED ON 1/2 BIT OFFSET QPSK			

Test configurations have been recommended for both the communications and the command and telemetry functions and they are discussed in Section 3. Since the actual tests are based upon DSCS III hardware, a discussion of DSCS III schedules and hardware availability is presented in paragraph 3.4. The costs for design and implementation of the simulator have been derived and submitted under separate cover.* A discussion of the design and hardware tradeoffs is given in Section 5. All elements to be developed, including hardware, firmware and software, are within the current state of the art.

* General Electric Space Division Proposal Number U80029 "Propagation Simulator Development", 8 February 1980.

SECTION 3
DSCS III MISSION CRITERIA AND ASSOCIATED TEST CONFIGURATIONS

3.1 PERFORMANCE CRITERIA, COMMUNICATIONS SUBSYSTEM

The DSCS-III Satellite SHF Communications Subsystem is a six channel non-processing transponder. Each of the six independent repeaters is capable of relaying telephony, data, wideband imagery and secure digital voice signals using FM, PSK, QPSK and frequency hopping PRN spread spectrum modulation. TDMA, FDMA, CDMA and SSMA users can be supported by any of the transponder channels. Linear, quasi-linear and saturated modes of operation are provided by means of selectable gain steps. Four synchronous geo-stationary satellites will be used to provide local area and wide area interconnection for the users of the Defense Communication System (DCS).

While some users will operate in FDMA or hybrid TDMA/FDMA modes, the overall trend is toward the increased use of digital modulation. Quantitative and repeatable performance definition of these digital modulation systems is determined by the Bit Error Rate (BER). In addition, this parameter can be related to both the ideal modem performance in both non-fading and in (flat) Rayleigh fading environments and to DSCS III nonfading transponder performance. A useful reference parameter is the Rayleigh mean (or median) Energy per bit to Noise-Density ratio, E_b/N_b. Because of its definitive nature and its repeatability, the Bit Error Rate will be the primary measure of communications performance. Test configurations discussed later in this section will be instrumented to measure the mean BER as a function of the mean E_b/N_o. Figure 1 illustrates the overall simulation concept and Table 1 specifies the maximum data rates for these tests.

In many cases, the BER measurement can be supplemented with the modem loss-of-lock indication, which is useful in burst-error analysis. Loss-of-lock in the SHF Telemetry downlink is an important performance element because the uplink and downlink COMSEC devices must be synchronized to insure satellite reception of valid commands.

3.2 PERFORMANCE CRITERIA, COMMAND AND TELEMETRY SUBSYSTEM

The X-Band command and telemetry links accept uplink encrypted commands and transmit downlink encrypted telemetry. Performance of the command link is dependent upon maintenance of crypto synch, which is a function of the telemetry link characteristics. Accordingly, three fundamental objectives are defined for the command link tests:

a. Determine the ability of the uplink to accept valid commands independently of downlink characteristics; e.g., the downlink signal level is sufficient to insure crypto synch.

b. Determine the error rate and the fade margins needed to ensure freedom from loss-of-lock on the Telemetry downlink.

c. Determine the ability of the uplink to accept valid commands as influenced by telemetry path (downlink) fading. Measurements to define those objectives can readily be made when the KI-24 is interconnected with the KT-42 test set. However, in the spacecraft configuration, the measurements will be less direct and more time consuming, especially items "b" and "c" above.

Command errors are reported in the downlink telemetry as BYTE ERRORS (Process of 2nd and sub-bytes), COMMAND ACCEPT and COMMAND REJECT. Acceptance of a command is contingent upon the successful processing of three bytes. Because the information bits are encoded in both the time and frequency domains, bit errors cannot be counted. Uplink performance will therefore need to be determined on the basis of the command reject rate and the link fade margin. This is a grosser performance monitor than the bit error rate criterion.

Errors in the downlink telemetry can be determined by means of an indirect process. These are relatively large block of telemetry data which remain unchanged unless the spacecraft is commanded. For example, the telemetry which describes the setting of the Variable Power Dividers in the three multibeam antennas (MBA's) is sampled six times per master telemetry frame. A master telemetry frame occurs once per 61.44 seconds. Decommutated MBA data can be stored and compared with data extracted from successive telemetry frames when the telemetry link is subject to fading. There will be approximately 780 bits for comparison in each minute, altogether too little data for measurement of significant error rates. Additional telemetry blocks such as that derived from the Jammer Location Electronics (126 Bits/Master frame) can be used to expand the data base. Monitoring of the Fill Data Alarm and the KG Alarm (loss of lock) should also be accomplished. The criteria for performance would be Bit Error Rate (up to about 1×10^{-4}) and frequency of loss-of-lock versus the available fade margin. Since loss of lock will occur at high bit error rates, the small data blocks should prove adequate. Since there are finite recovery times associated with the loss-of-lock, the corresponding burst error lengths should be accounted for.

3.3 TEST CONFIGURATIONS

3.3.1 SHF Command Link Test Configurations

SHF Command Link fading simulations may be conducted in the test configuration shown, in Figure 2. In the configuration shown, the fading simulator requires an S-Band input capability and an X-Band output capability. Processing of the signal will occur at a more convenient lower frequency, 700 MHz.

The S-Band Command signals are generated in the KT-42 test set. If the DSCS III SHF communications subsystem is in the systems test configuration, the simulator may be interfaced to the satellite at 700 MHz using an upconverter which is part of an existing X-Band Interface Rack, an item of General Electric test equipment.

Demodulation occurs in the telemetry receiver; the receiver output is cypher-text telemetry, which is applied to the input port of the KT-42 test set. In this configuration, the KT-42 cannot perform error counts on the decrypted telemetry, although plain-text telemetry generated in the KT-42 can be used for checking of its internal downlink circuits. The KG Alarm should be monitored to determine when loss of synch occurs. When the KT-42 can be cabled directly to the satellite COMSEC device (a KI-24) the KT-42 is capable of performing telemetry bit-error-rate counts. Counting of errors is then accomplished by having the KT-42 generate and provide a plain text telemetry signal to the KI-24, which encrypts the signal and returns it to the KT-42. The KT-42 decrypts the signal and compares it to the original plain-text telemetry sent to the KI-24 and determines the error rate. A test configuration that provides this capability is shown in Figure 3. It's

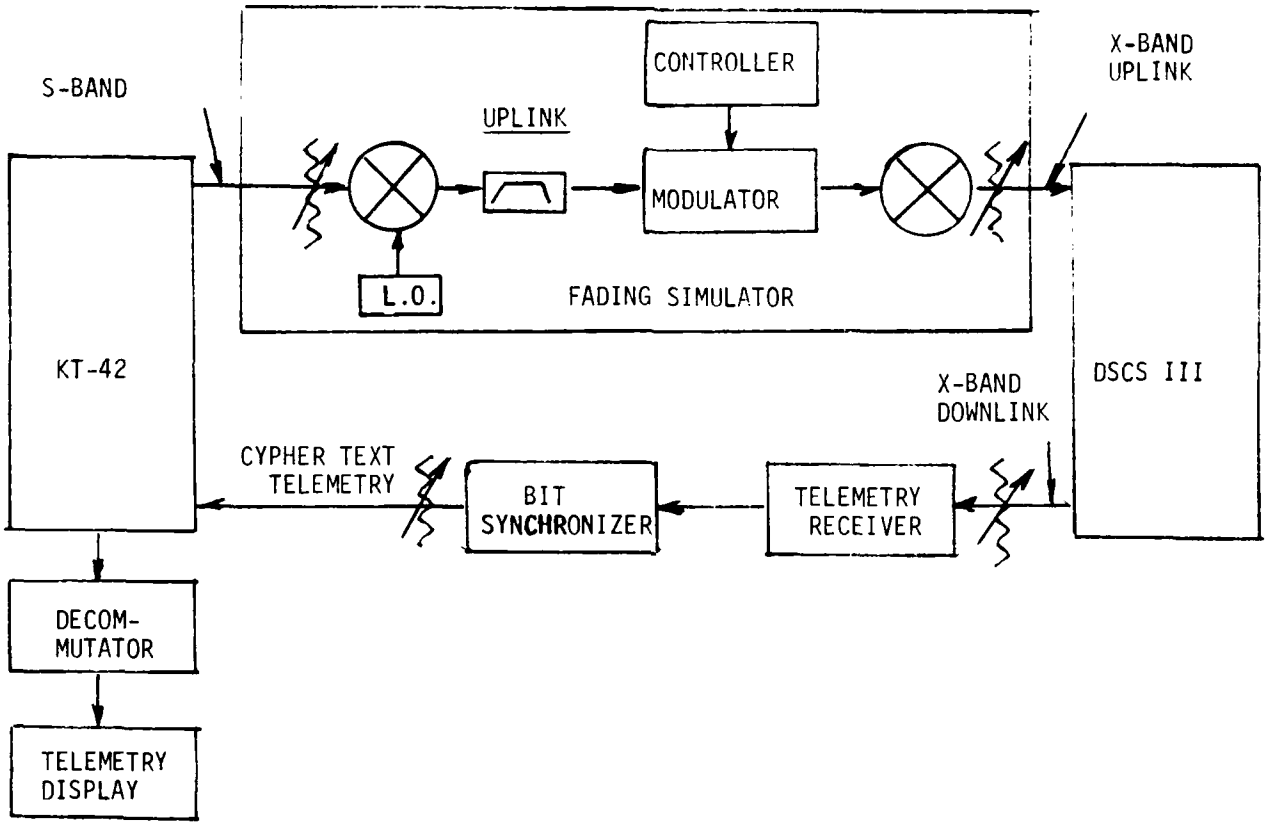

Figure 2. SHF command link test configuration.

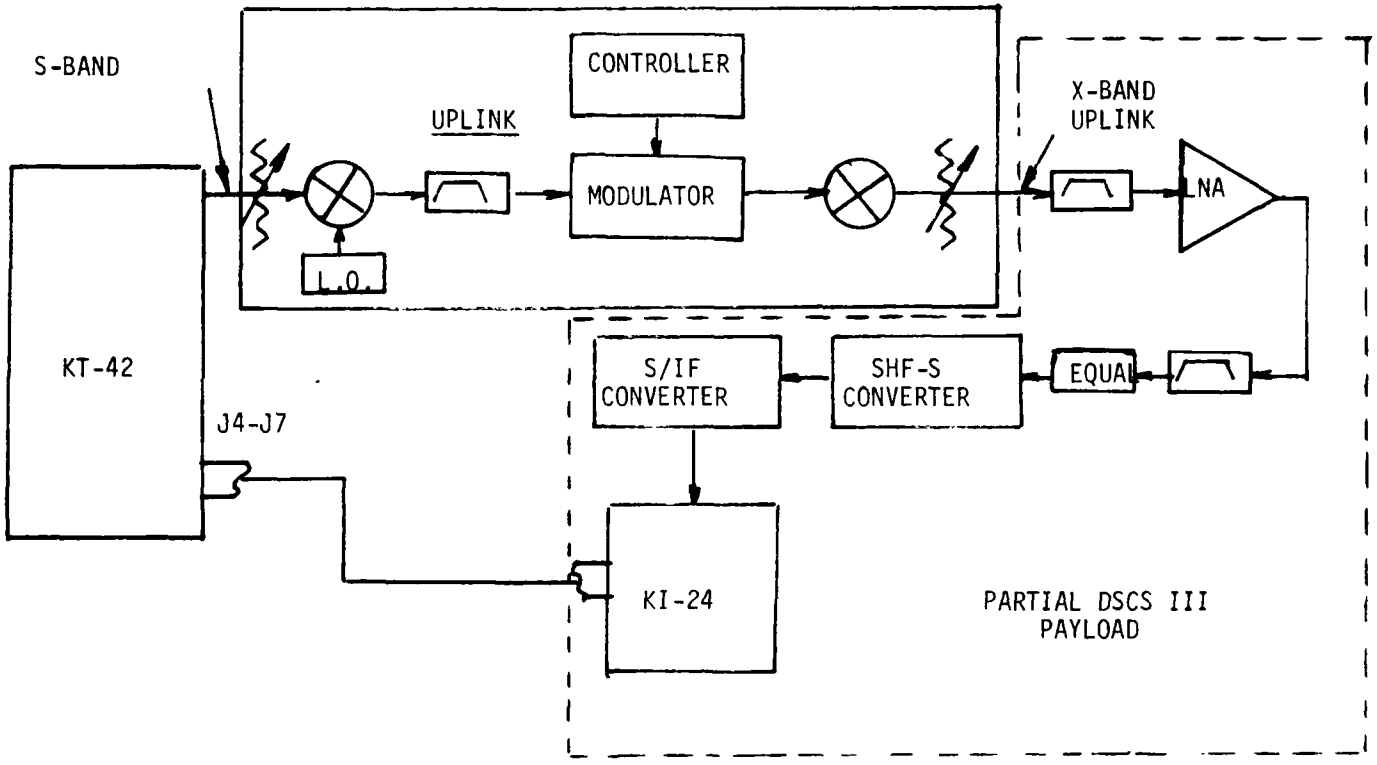

Figure 3. Alternative command link test configuration.

principal drawback is that it excludes the Telemetry transmitter and receiver and therefore, the performance as a function of fade margin cannot be determined. However, it does permit definitive telemetry Bit Error Rate date which can be used for reference.

3.3.2 Communications Link Test Configurations

Communications link testing is expected to occur at Ft. Monmouth, N.J. and at Ft. Detrick, Md. Communications interfaces are required for interconnection with the following items of equipment:

a. The DSCS III SHF Communications Subsystem

b. The DSCS III SHF Communications Simulator

c. S.H.F. Earth terminal up and downconverters (Heavy terminal/ Medium Terminal) and the HT/MT Simulator

d. Modems having a 700 MHZ interface.

These interfaces are described in detail in Section 5.

A test configuration that utilizes on-site up and down-converters is shown-converters is shown in Figure 4. This configuration provides complete flexibility when interconnecting to an existing facility, using flexible coaxial cable. An uplink simulation is shown. For a downlink simulation, the propagation simulator would be connected between the downconverter and the demodulator.

Satellite level or communications panel level testing at the Valley Forge assembly area may also be feasible. In this case the test configuration would be virtually identical to the field test configuration, substituting DSCS III test equipment for interfacing between the satellite communications payload and the simulation equipment. This configuration is given in Figure 5.

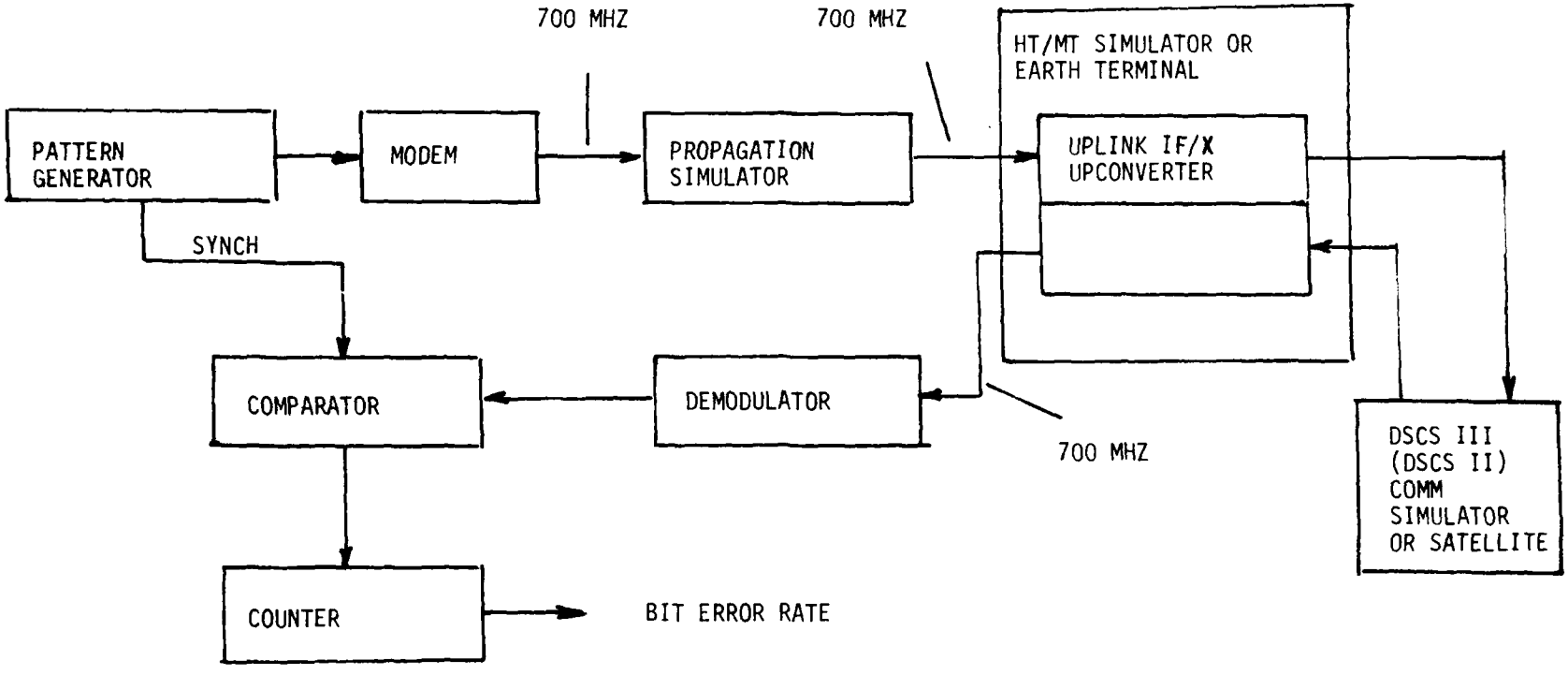

Figure 4. Communications link test configuration - SATCOMA, Ft. Monmouth, N.J. and Ft. Detrick, Md.

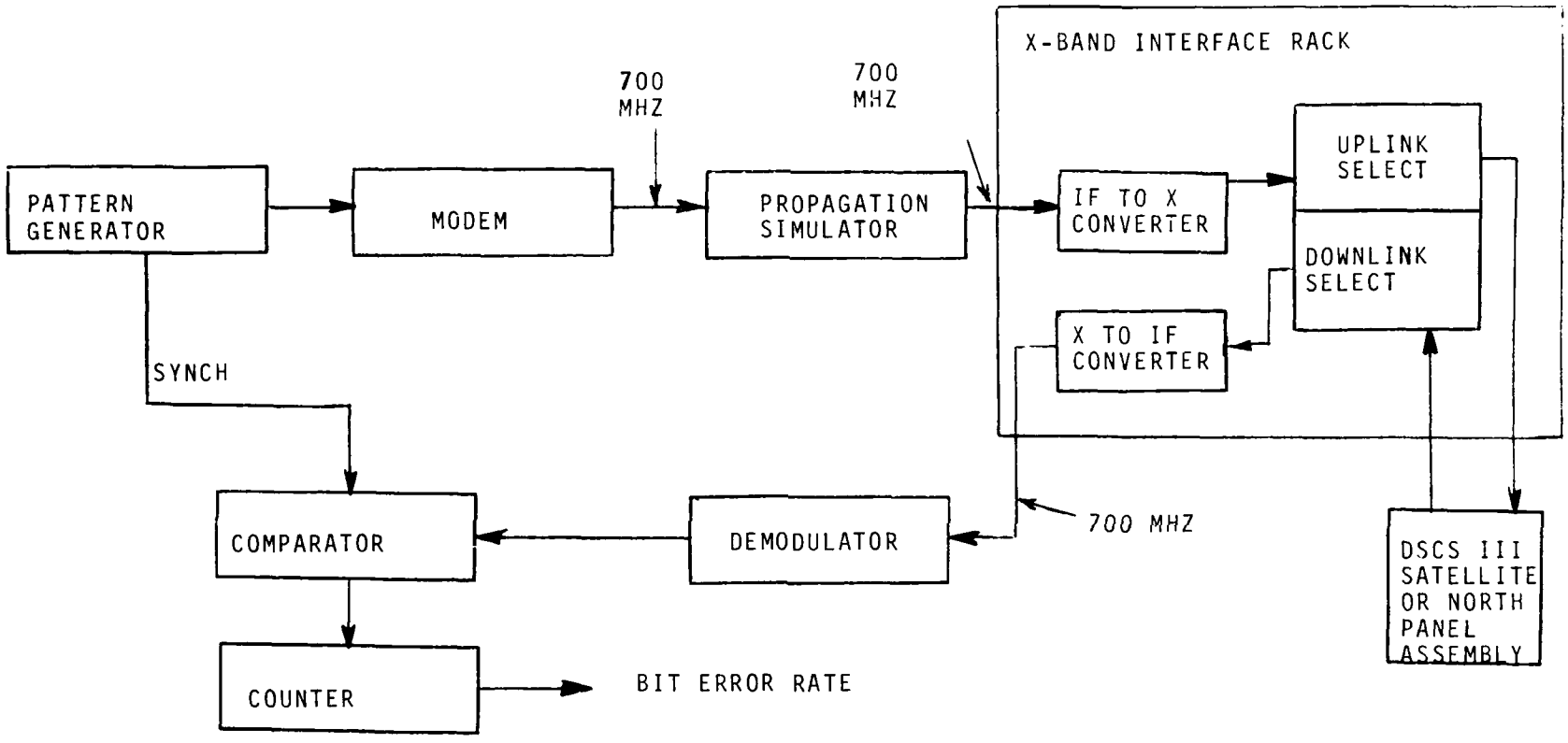

Figure 5. Communications link test configuration - Valley Forge, Pa.

3.4 SELECTION OF HARDWARE AND DSCS III SCHEDULES

The feasibility of establishing specific test conditions is dependent upon the availability of DSCS III hardware. Selection of DSCS III hardware to be tested is based upon the following units, in descending priority:

a. Qualification Hardware

b. Engineering Models

c. Breadboard Hardware

Fabrication, assembly and integration and test status of the qualification and first two flight satellites is presented in the Master Schedule of Figure 6. Testing of the Qualification Vehicle is feasible in January or February 1981,(all testing is contingent upon approval of the DSCS III Program Office). After completion of the Qualification Satellite and evaluation of the test data, the unit may be refurbished for launch. Refurbishment, assembly, integration and test of the Qualification Satellite is expected to be completed in early 1983.

Enginering Model Hardware has been used to construct a DSCS III Communications Simulator. This simulator will be delivered to the SATCOMA Simulation Facility 45 days prior to launch of the first flight vehicle, or approximately 1 February 1981.

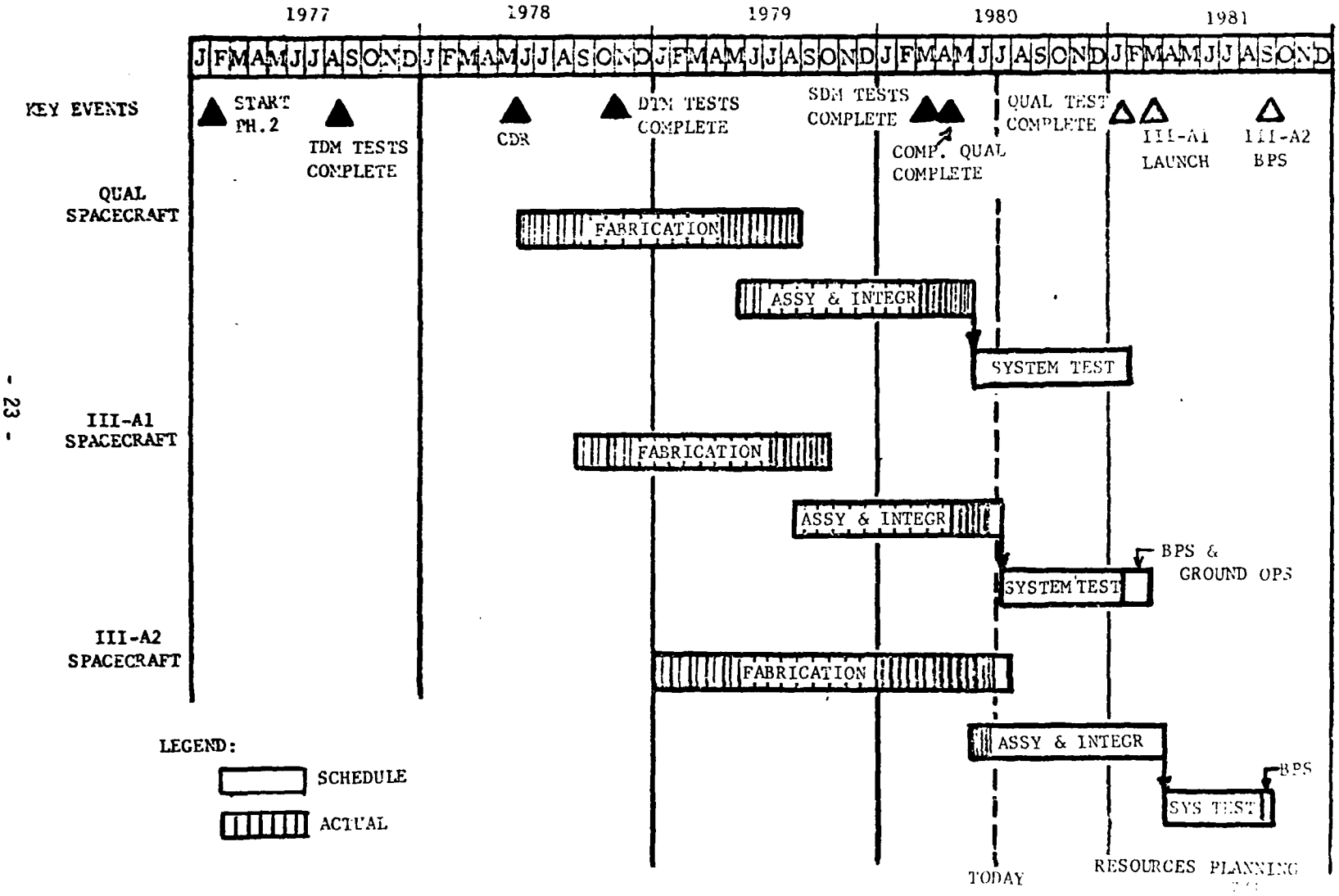

Figure 6. DSCS III Phase 2 master schedule.

Prior to the development of the engineering model, a breadboard model was fabricated. The breadboard was essentially a single channel repeater that was used to validate critical design and performance requirements. Breadboard components have been absorbed to some extent in the Engineering Model.

Use of the DSCS-III Communications Simulator, which will be installed at the USASATCOMA Simulation Facility in Ft. Monmouth, N.J. is tantamount to using the Engineering Model Hardware. Since the DSCS-III communications simulator will not have either the COMSEC device (BATSON I or II) or a telemetry subsystem it cannot be used for command link tests. Command link tests can be performed on either the Qualification or the first two flight vehicles using BATSON I, or on the succeeding Phase 3 vehicles, which use the BATSON II COMSEC device. Phase 3 vehicle production has not yet been placed under contract.

Such testing must occur on a non-interfering basis with the DSCS III schedule. Reference to the typical assembly and test schedule appearing in Figure 7 shows that approximately nine months is required to complete the assembly and test cycle.

The only period of time in which any of the vehicle remain in one configuration for relatively long periods of dead time is during the thermal balance and thermal vacuum test period. During these tests the vehicle is interconnected to a facility having the same command generation and telemetry decommutation and readout capability that exists in a control terminal.

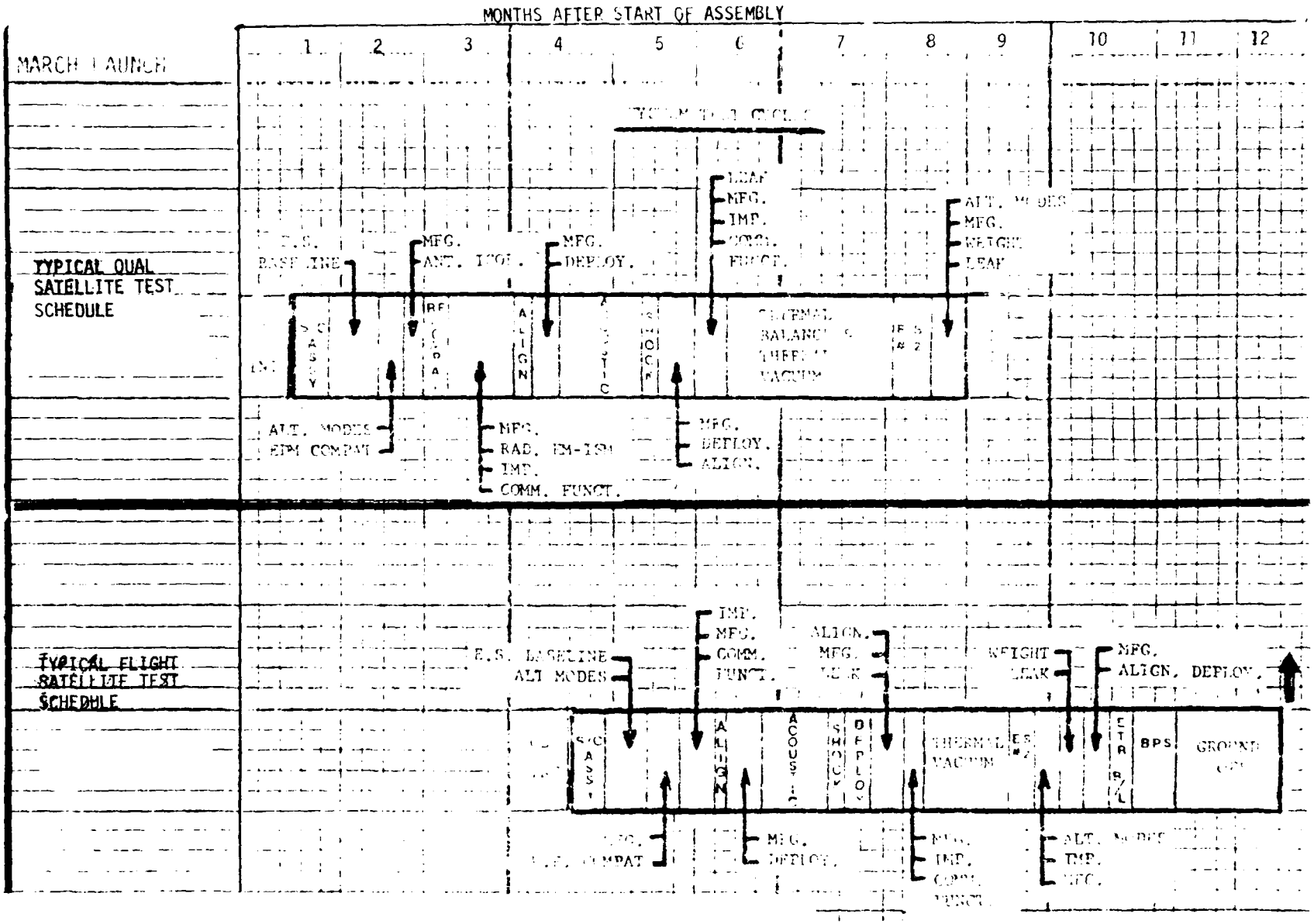

Figure 7. Typical vehicle assembly and test schedule.

3.5 SUMMARY OF TEST AND HARDWARE REQUIREMENTS

Test requirements and hardware assets that have been discussed are summarized in Table 2. Both linear and saturated communications modes should be tested on the basis uplink and downlink simulations. Modems used for this test should include the following:

- General Electric,QPSK (1.33 Bits/Hz) - This modem provides an assessment of performance of high speed data transmission in non-fading and fading environments, similar to DSCS wideband users.
- AN/USC-28 - This unit provides an assessment of spread-spectrum modem performance in fading and non-fading environment.
- TDMA Modem - As available on a GFE basis.

Availability of specific modems is to be negotiated with the principals as the plans and procedures are developed.

The SHF command links also require uplink and downlink simulations. Uplink simulations will determine the necessary margins required to maintain the specified command reject rate while the downlink simulations are required to determine the margins needed to maintain crypto synch. Hardware assets needed to perform these simulations are identified in Figures 2, 4 and 5. The fading simulator does not exist and is an item to be built. Basic design criteria and implementation methods are established in Sections 4 and 5.

Table 2. Summary of test requirements.

FUNCTIONS TO BE TESTED (1)	EVALUATION CRITERIA	TEST CONFIGURATIONS	HARDWARE ASSETS REQUIREMENTS
COMMUNICATIONS			
o LINEAR MODE	BER $\leq 1 \times 10^{-6}$ BITS/BIT	FIGURE 3.4	FIGURES 4-5
o SATURATED MODE	BER $\leq 1 \times 10^{-6}$ BITS/BIT	FIGURE 3.4	FIGURES 4,5
SHF COMMAND LINK			
o ABILITY TO COMMAND SPACECRAFT	COMMAND REJECT RATE $\leq$ (2)	FIGURE 2	FIGURE 2
o LOSS OF LOCK ON DOWNLINK TELEMETRY	FADE MARGIN, TO BE ESTABLISHED BY TEST, WITH LIMITED BIT ERROR RATE DATA	FIGURE 2	FIGURE 2, SIMULATOR IN DOWNLINK

(1) UPLINK AND DOWNLINK SIMULATIONS ARE REQUIRED FOR BOTH COMMUNICATIONS AND THE COMMAND LINKS

(2) VALUE IS OMITTED SINCE IT IS CLASSIFIED

SECTION 4
THEORETICAL BACKGROUND AND DEVELOPMENT OF SIMULATION REQUIREMENTS

Accurate reproduction of atmospheric fading phenomena requires a sound mathematical model of the trans-ionspheric satellite channel and a suitable device for implementing the simulation. A tapped delay line with time-varying tap weights has been chosen as a suitable device for reproducing the statistical channel model provided to the Space Division of General Electric by the Defense Nuclear Agency. Fixed parameters of the delay line such as tap spacing and total line length are selected to allow simulation of predicted worst-case fading conditions. Modern digital signal processing techniques provide a flexible means of generating both worst-case and less severe fading envelopes for use as the tap weighting functions.

4.1 SUMMARY OF FADING STATISTICS

The nuclear-disturbed ionosphere is predicted to have dense and irregular field-aligned concentrations of ions. The time-varying instabilities of these irregularities causes the principal radio signal to be broken into many weak components, each component suffering varying amounts of phase shift and attenuation. If each component has a uniform phase probability distribution, the recombined signal envelope at the receiving antenna will be Rayleigh amplitude distributed. The Rayleigh amplitude assumption is made for all operations of the propagation simulator.

Determination of the amplitude distribution does not determine in what way the amplitude changes as a function of time. For this purpose the time autocorrelation function is defined as:

$$R_H(\Delta t) = \tfrac{1}{2}\int H^*(j\omega,t)H(j\omega,t+\Delta t)dt, \qquad (1)$$

where $H(j\omega,t)$ is the (time-varying) channel transfer function for the signal envelope.

If the narrow band restriction is removed, then one spectral component of the signal may fade with a different envelope than a component at a different frequency in the band. If the mean power across the band remains constant in time, the frequency autocorrelation function

$$R_H(\Delta\omega) = \tfrac{1}{2}\int H^*(j\omega,t)H(j(\omega+\Delta\omega),t)d\omega \qquad (2)$$

and the Rayleigh amplitude assumption are sufficient to define the "frequency selective" fading case.

In general, both time and frequency selective effects can be expected. Then, the joint autocorrelation function

$$R(\Delta\omega,\Delta t) = \tfrac{1}{2}\iint H^*(j\omega,t)H(j(\omega+\Delta\omega),t+\Delta t)d\omega dt \qquad (3)$$

and the Rayleigh assumption define the channel. A more useform form of (3) is its Fourier transform, which is sometimes called the channel scattering function:

$$S(\tau,f) = \iint R(\Delta\omega,\Delta t)e^{j\Delta\omega\tau}e^{-jf\Delta t}d(\Delta t)d(\Delta\omega) \qquad (4)$$

The scattering function has a physical interpretation similar to the familar ambiguity function used in radar system analysis. The variable τ represents delay. An ideal channel would pass a pulse with a constant delay. Similarly, the variable f represents frequency, and a pulse of constant frequency should be received as a constant frequency. The ideal channel therefore has an impulse scattering function, the impulse being centered at the nominal group delay and carrier frequency. Usually the scattering function origin is taken as the location of this impulse. The scattering function of a non-ideal channel will be spread in frequency if the average received power is a random process (time-selective fading) and will be spread in delay if the channel frequency response is a random process (frequency selective fading). In general, $S(\tau,f)$ is a surface above the τ,f plane. Finally, it can be stated that the marginal distributions $S(f)$ and $S(\tau)$ are the power spectral densities of the time response and frequency response random processes, respectively. Henceforth, the term "flat fading" shall refer to the time-selective-only distribution $S(\tau,f) = S(f)\,\delta(\tau)$, , while "frequency selective" fading will encompass the joint distribution $S(\tau,f)$.

4.2 DSCS-III CHANNEL DESCRIPTION

The nuclear-disturbed channel is predicted by the Defense Nuclear Agency* to have the following scattering function (See Appendix I).

*L.W. Wittwer, Unpublished Memorandum, "The Statistical Reconstruction of Scintillated Signals", April 1, 1979.

$$S(k_\rho, \tau) = \left(\begin{array}{l} \pi^{\frac{1}{2}} l_o^2 \, (f_c/\sigma_\phi^2)^{\frac{1}{2}} \exp(-k_\rho^2 l_o^2/4) \\ \cdot \exp\left\{-(k_\rho^2 l_o^2/4f' + 2\pi\tau)^2 \, (f_c^2/2\sigma_\phi^2)\right\} \\ \cdot \gamma/B \exp(\gamma^4/2B^2) \quad K_{\frac{1}{4}} \, (\gamma^2/2B^2) \end{array} \right) \qquad (5)$$

where

f_c = carrier frequency

$K_{\frac{1}{4}}$ = Bessel function of third kind (see Appendix 1)

l_o = Decorrelation distance

f_o = frequency selective or correlation bandwidth

σ_ϕ^2 = integrated phase variance

$\gamma^2 = l_o^2(1 + f_c^2/(f'^2 \sigma_\phi^2) \cdot (k_\rho^2 l_o^2 + 2\pi f'\tau))/8$

$B^2 = (l_o^2/4f')^2 \, (f_c^2/2\sigma_\phi^2)$

Note the use of k_ρ as an independent variable. The wave number k_ρ is related to the frequency shift f used previously as

$$k_\rho = 2\pi f/V$$

where v is the relative velocity of the ion cloud with respect to the receiver. Another critical relationship to be considered in the simulation is the decorrelation time, defined by the following expression:

$$\tau_o = \text{decorrelation time} = l_o/V \qquad (6)$$

The DSCS III scattering function is difficult to visualize directly from the equation, so a three-dimensional plot of it is presented in Figure 8. The parameters used are for the predicted worst case, in the sense that they use the highest fading frequencies and the longest delay spreading expected. Note the scalloped effect in the wings of the illustrated scattering function. This effect is due to the width of the function being comparable to the grid spacing capability of the plotting routine. In reality, the function decays smoothly according to an exponential law.

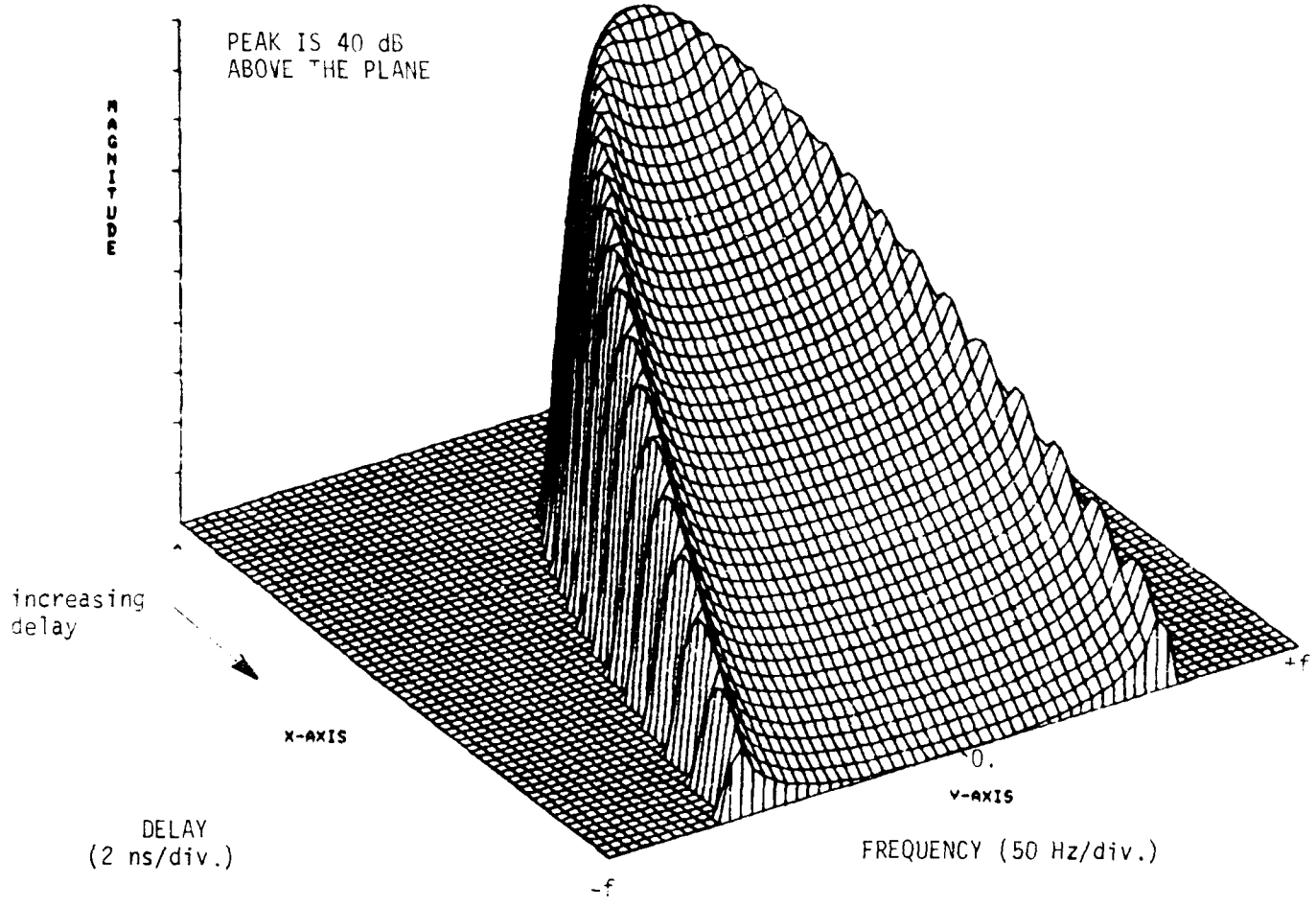

Figure 8. Three dimensional view of DSCS-III channel scattering function.

4.3 DEVELOPMENT OF SIMULATOR REQUIREMENTS

The basic requirement of the propagation simulator is that a fading environment be produced such that the fading envelope be a random process having a Rayleigh amplitude distribution and a joint spectral density defined by the scattering function of Equation (5). A tapped delay line meets this requirement by forcing the tap weights to be time functions derived from the scattering function statistics.

A perfect simulator would have infinitely many taps spaced at infinitesimal intervals, each tap being modulated by an analog waveform having the power spectrum determined by the intersection of the scattering function and a plane normal to the delay axis at the delay of the tap.

An approximation to the perfect simulator involves quantization of both the tap spacing and the tap weight modulating functions. Each modulating function is the filtered output of a digital-to-analog converter being driven by a digital computer. The computer stores enough modulating data in memory to provide a statistically significant test time. For longer tests, the data may be repeated cyclically.

Figure 9 shows the tapped delay line concept and the tap modulators. The signal from each tap will power-split into an in-phase and quadrature signal, each being modulated by an independent Gaussian process. The sum of the modulated in-phase and quadrature signals is Rayleigh distributed with uniform phase. This technique is much simpler than trying to implement Rayleigh fading and a uniform phase shift directly, because the amplitude and phase functions are not independent.

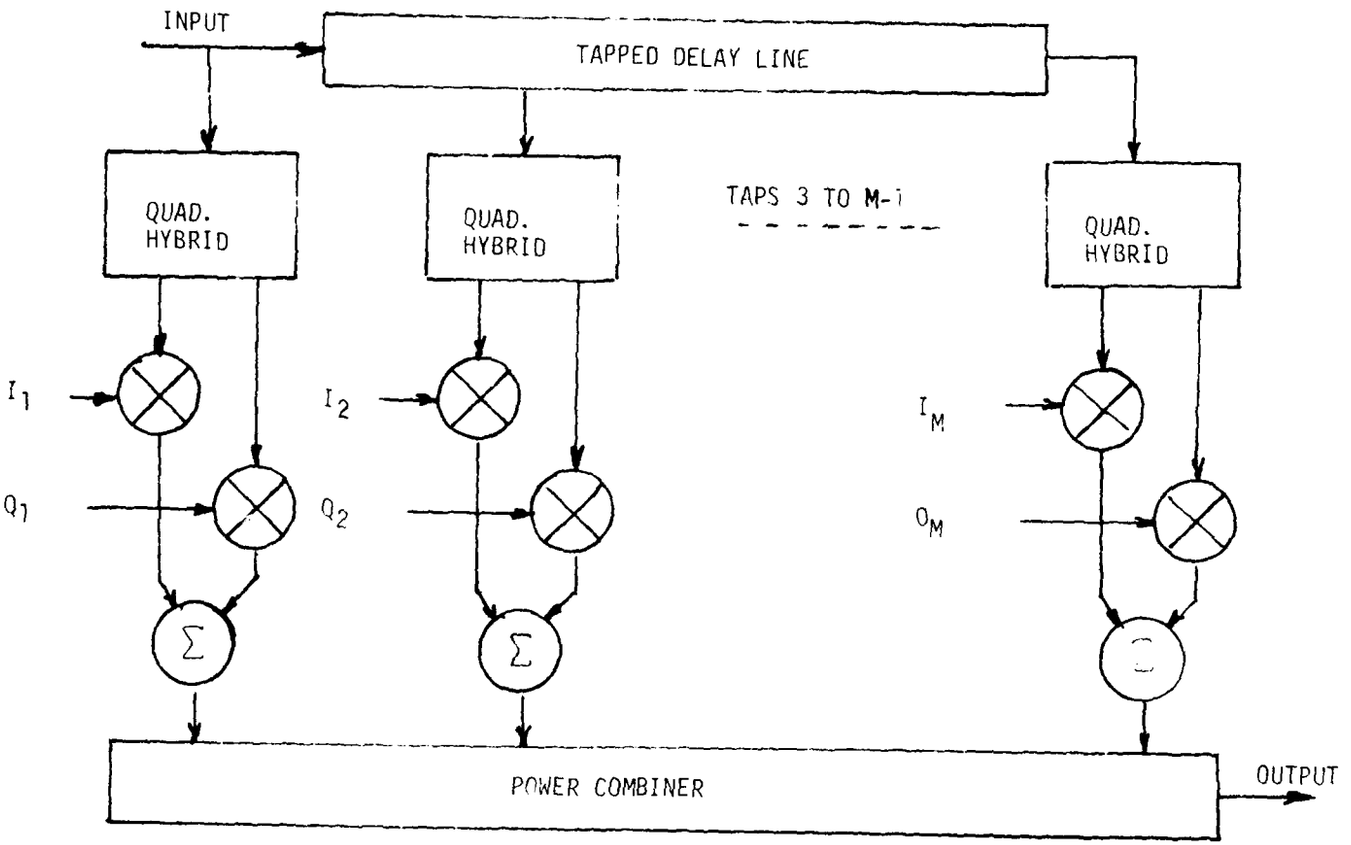

Figure 9. Tapped delay line showing in-phase and quadrature modulation. Tap modulating functions I and Q are analog waveforms resulting from D/A conversion of IFFT generated sequences.

The important parameters of the delay line (Table 3) have been chosen using a combination of analysis and good engineering judgment.

The delay line length and highest fading frequency can be determined by truncation of the scattering function such that 99.9 of the fading energy is within the length of the line and below the highest frequency. More details are provided in Appendix II. The tap spacing has been chosen to provide a reasonably accurate reproduction of the power delay spread. For the frequency selective fading test, the 40 MHz bit rate corresponds to a 25 ns bit period. At least 10 taps per bit period was deemed sufficient (see reference of para. 4.2) hence the spacing was set at 2 ns between taps.

The fading bandwidth is proportional to the inverse of the decorrelation time, τ_o . The Nyquist condition requires that the number of D/A samples per second exceed twice the fading bandwidth. However, the output of the D/A contains not only the desired fading spectrum but harmonics of this spectrum at multiples of the D/A rate. For the maximum fading rate, these harmonics will be rejected by a fixed lowpass filter, and the D/A rate will be Nyquist (about 2,000 samples/sec.). For longer τ_o and consequently lower fading bandwidths, the D/A rate will be about $10\ \tau_o^{-1}$, or five times the Nyquist rate. This rate avoids the necessity of a variable-cutoff lowpass filter, and reduces in-band distortion and out-of-band interference to an acceptable level (see Appendix III).

Table 3. Delay line and digital controller requirements.

PARAMETER	FREQUENCY - FLAT FADING SIMULATOR (SINGLE TAP)	FREQUENCY SELECTIVE FADING SIMULATOR (MULTIPLE TAPS)
Delay Line Length (ns)	Not Applicable	100
No. of Taps	1	50
Tap Spacing (ns)	N/A	2
Range of Decorrelation Time, τ_o (sec)	0.001 - 13.0	0.001 - 13.0
Range of Highest Fading Frequency (HZ)	1,000 - 0.08	1,000 - 0.08
Highest D/A Update Rate (HZ)	2,000	2,000
Minimum Data Record Length (Sec)	$100\tau_o$ *	$100\tau_o$*
D/A Quantization (Bits)	8	8
Modulator Dynamic Range (dB)	35	35
CPU Memory Size (Kilobytes)	64	256

* Design Goal is 200

Eight-bit logarithmic D/A converters (seven bits plus sign) will provide a 0.27 dB resolution over the nominal 35 dB modulator dynamic range. This resolution is more than sufficient. Modulator dynamic range requirements are discussed in greater detail in paragraph 5.3.2.

4.4 ALGORITHM FOR TAP WEIGHTING FUNCTION GENERATION

A tapped delay line with time-varying coefficients will be used to reproduce the statistics of the scattering function (para. 4.2) in the following manner.

4.4.1 Time Selective Fading

First, consider the case of the time selective fading only. The scattering function is therefore zero everywhere except where (delay) = 0. What remains is a power spectral density in the variable k_ρ, and the delay line reduces simply to one tap having zero delay. The fading envelope is now the tap modulating function, which can be expanded in the Fourier series approximation as

$$x(t) = 1/T \sum_{n=-N}^{N} c_n \exp(jn\frac{2\pi}{T} t)dt. \tag{7}$$

The signal $x(t)$ is assumed to be a periodic Gaussian random process, so that the Fourier coefficients c_n are independent complex random variables, with Gaussian distributed real and imaginary parts. The variance of either the real or imaginary distribution of c_n is given by

$$\sigma_{c_n}^2 = \overline{c_n^* c_n} = T\int_{(n-\frac{1}{2})2\pi/T}^{(n+\frac{1}{2})2\pi/T} \int_{-\infty}^{\infty} S(k_\rho, \tau)\, d\tau\, dk_\rho. \tag{8}$$

Thus the procedure to produce the amplitude function for the one-tap flat fading case is to choose a test length T in seconds, integrate the scattering function over small intervals spaced at $2\pi/T$ radians to obtain the σ_{c_n}'s, then form the summation (7) with coefficients c_n chosen at random from the corresponding Gaussian distribution having variance . The summation limit N is chosen high enough to include all significant values of S in the integral (8).

While the summation (7) will produce the function $x(t)$ for all t, only samples of $x(t)$ at intervals spaced at T/N seconds are really needed. If these N time samples are used to produce the waveform

$$\tilde{x}(t) = x_n \, p(t-nT/n)$$

where

$$p(t) = \begin{cases} 1 & 0 \le t \le T/N \\ 0 & \text{elsewhere} \end{cases} \qquad (9)$$

and $\tilde{x}(t)$ is low pass filtered, then the resultant waveform will approximate $x(t)$. The sampling process greatly reduces the computation of (7), because the sampled function expansion

$$x(t_i) = 1/T \sum_n c_n \exp(jn \tfrac{2\pi}{T} t_i) \qquad (10)$$

can be recognized as an inverse discrete Fourier transform (IDFT), which will be implemented as an inverse fast Fourier transform using N equal to a power of 2.

4.4.2 Time and Frequency Selective Fading

Now consider the more general case of both time and frequency selecting fading. The marginal density $S(\tau)$ can be obtained by integration

$$S(\tau) = \int_{-\infty}^{\infty} S(k_\rho, \tau) dk_\rho \quad . \tag{11}$$

This provides the power density as a function of delay. An example is shown in Figure 10. By segmenting this curve into M portions, the integral over each delay element becomes the average power in the corresponding tap of a delay line. The amplitude function of the tap apportions this average power into various modulating frequencies in accordance with the power spectral density for that tap. More precisely, the psd of the m^{th} tap is

$$S(k_\rho, \tau_m) = \int_{\tau_m - \Delta\tau/2}^{\tau_m + \Delta\tau/2} S(k_\rho, \tau) d\tau \, , \tag{12}$$

where $\Delta\tau$ is the tap spacing of 2 ns. M is a function of f_0, the frequency selective bandwidth and is chosen to include all significant energy in S.

The tap weight generating procedure for the multiple tap case is now only slightly more complex than the single tap. Instead of generating one frequency-sampled length N sequence and digitally transforming it into a length N time sequence, there are M such sequences, one for each tap. The m^{th} tap sequence is the output of the FFT

$$A_m(t_i) = 1/T \sum_n c_n(\tau_m) \exp(jn\frac{2\pi}{T} t_i) \quad , \tag{13}$$

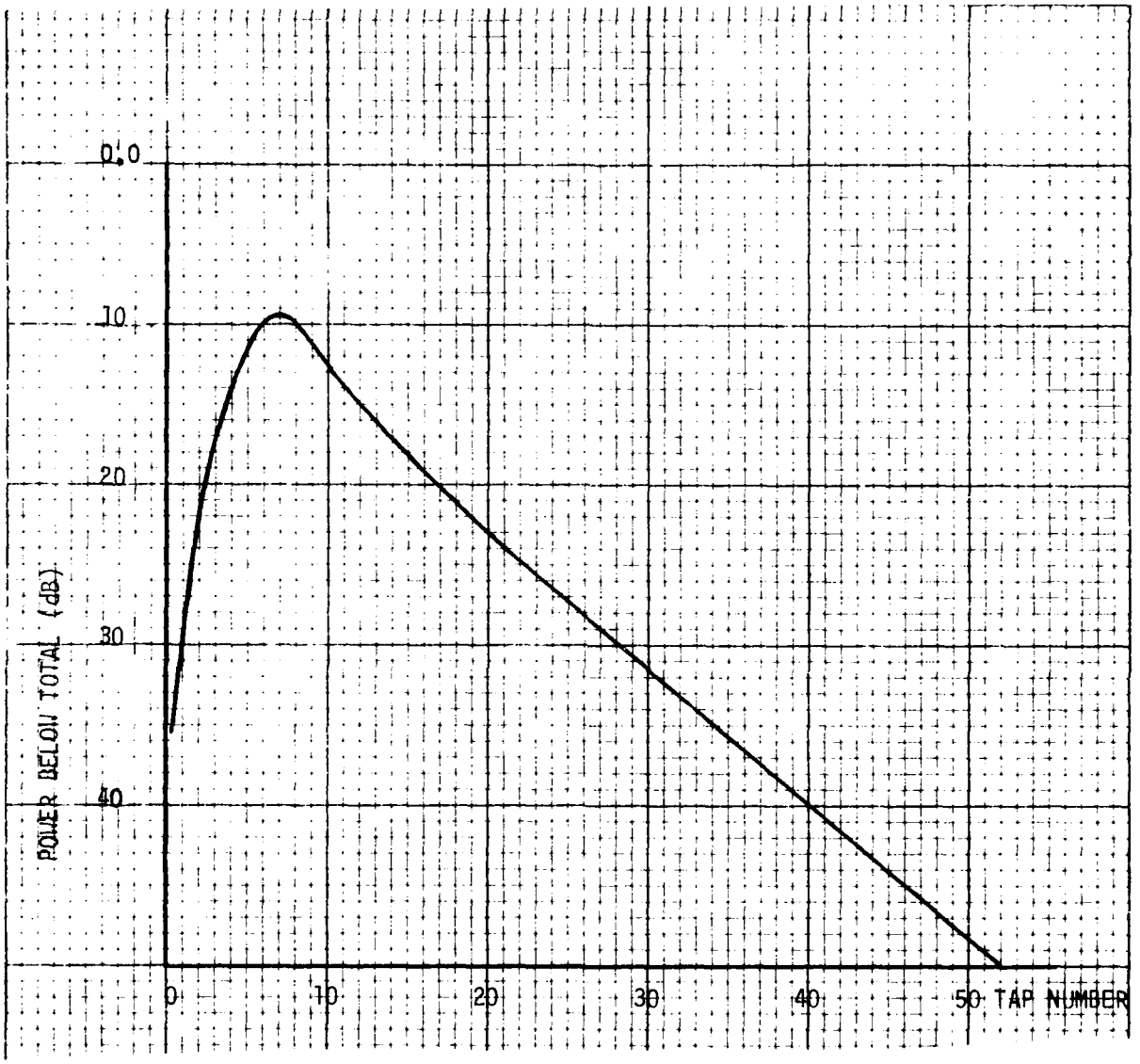

Figure 10. Marginal power spectral density as a function of delay. Curve is obtained by intergration of the channel scattering function over the frequency variable. Taps are spaced at two nanoseconds.

where the N values $c_n(\tau_m)$ are complex samples from Gaussian distributions having variances by

$$\begin{aligned}
\sigma^2_{c_n(\tau_m)} &= \overline{c_n^*(\tau_m)c_n(\tau_m)} \\
&= T\int_{(n-\frac{1}{2})2\pi/T}^{(n+\frac{1}{2})2\pi/T} S(k_\rho, \tau_m)dk \\
&= T\int_{\tau_m-\Delta\tau/2}^{\tau_m+\Delta\tau/2}\int_{(n-\frac{1}{2})2\pi/T}^{(n+\frac{1}{2})2\pi/T} S(k_\rho, \tau)dk_\rho d\tau \quad .
\end{aligned} \tag{14}$$

Figure 11 is a flowchart of this process.

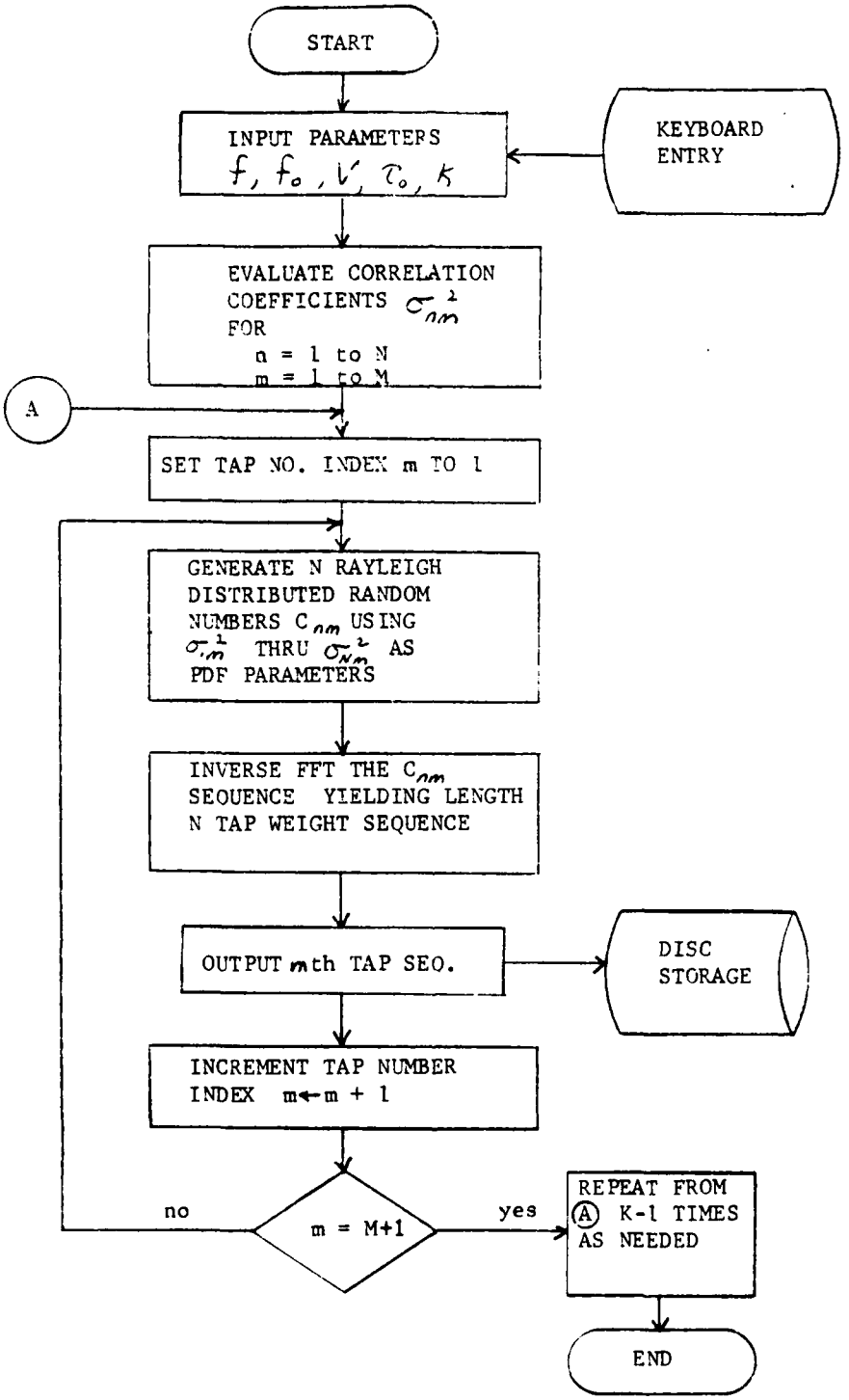

Figure 11. Offline processing of tap weight sequences.

4.5 SIMULATOR SOFTWARE REQUIREMENTS

Due to the complexity of the algorithm used, the tap weighting data for each fading experiment will be generated off-line. The following additional off-line modules require development.

- Parameter entry and initialization
- Scattering function integration
- Gaussian random no. generator
- Fast Fourier transform
- Disk Input-Output

The scattering function integration module is for evaluation of Equation (7) for the flat fading case and (13) for the frequency selective case. Device non-linearity correction is related to the particular modulators chosen: these are non-linear due to both drive current and input power fluctuations. Scaling refers to the conversion of floating point samples into properly scaled fixed-point numbers for use by the D/A converters.

The last module which requires explanation is the module for data block interpolation. If more than one N-point FFT is needed to satisfy the data requirement for a given tap, then an algorithm must be specified for maintaining at least first order correlation statistics between data blocks. The following equation* provides interpolated samples between two blocks X and with less than 10% correlation error at the decorrelation distance.

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* "Dual Modem (LES Mode) Experimental Test with Scintillated Signal Structures Final Technical Report", Linkabit Co., September, 1978.

$$s_m = x_{-m} \cos\left(\frac{\pi m}{2cR}\right) + y_{(2cR-m)} \sin\left(\frac{\pi m}{2cR}\right) \qquad (15)$$

$$1 \leq m \leq cR-1 \quad .$$

In equation (15) s_1 is the first point following the X data block, and s_{cR-1} is the point directly preceeding the Y data block. Also, x_0 is the last point of the X block, x_{-1} is the second to last, and y_{cR} is the first point in Y. The term cR is the product of the decorrelation distance R and a constant c which is chosen to minimize the number of interpolated points while minimizing correlation errors. A compromise value is c = 4 R.

SECTION 5
SIMULATOR DESIGN AND IMPLEMENTATION

The propagation simulator proposed by the General Electric Company accepts signals that are similar to those received and transmitted by the DSCS III SHF Command and Communication Subsystems. These signals are modified by means of digital and analog signal processing techniques which collectively simulate the passage of these signals through a spatially inhomogeneous and disturbed ionsphere, resulting in an output signal having Rayleigh statistics, as described in subsection 4.1.

Modelling of the disturbed ionsphere is accomplished by means of a time-varying linear filter implemented in the form of a densley-tapped delay line having provisions for amplitude and phase modulation ($0 - 2\pi$) at each tap. Since the output process is Rayleigh, it can be generated from in-phase and quadrature components of a random Gaussian process. As a practical implementation, the outputs of two independent Gaussian random processes are sampled and these samples are then processed to form variable amplitude weights which are applied to in-phase (I) and quadrature (Q) modulators at each delay line tap. Generation of the encoded tap weight data representing fading depth and fading frequency will occur at an off-line facility. Transfer of the encoded fading structure to the desired location for the simulation may best be accomplished with a removable medium (a flexible disk).

To perform the functions of simulation while interconnected to the DSCS-III subsystems, earth terminal equipment and modems, the simulator design has evolved into two major subsystems -

- The R.F./I.F. Subsystem
- The digital Controller Subsystem

The R.F./I.F. subsystem provides interconnectivity with the system elements to be evaluated and also contains the analog signal processing elements of the simulator. Digital processing and the software control elements reside within the Digital Controller subsystem which interfaces with the R.F./I.F. subsystem at the tapped delay line modulators of the I.F. Processor.

The recommended design is capable of being implemented initially as a flat-fading simulator (single-tap delay line) with capability for expansion to frequency selective fading later (50 tap delay line).

5.1 APPLICATIONS AND INTERFACE REQUIREMENTS

The R.F./I.F. subsystem provides input and output frequencies, power levels, impedances and connectors that insure compatible test configurations and simulations with the following DSCS III related items of equipment:

- DSCS III SHF Command and Telemetry Subsystem, with external converter
- DSCS III Communications Simulator to be installed at SATCOMA, through the HT/MT Simulator
- HT/MT Earth Station, at Ft. Detrick, Md.
- A variety of spread spectrum and standard modems having an I.F. interface at 700 MHz.

Flexibility in the test and simulation configurations is assured by providing for direct interconnection at 700 MHz to X-Band converters. Non-fading, and flat Rayleigh fading conditions can be imposed. In addition, provisions are made to inject additive noise to set specific mean values of E_b/N_0 and thereby establish modem performance as a function of margin to threshold in specific fading regimes.

The simulator gain distribution is compatible with the R.F. power levels listed in Table 4 and the I.F. power levels listed in Table 5. These are the interface levels for the simulation facility of SATCOMA (Ft. Monmouth, N.J.), actual earth terminals of the HT/MT class, the DSCS III payloads and for direct modem interfacing.

Table 4. X-band interface level.

INTERFACE TYPE	FREQUENCY BAND	REQUIRED LEVELS (dBm) P1 (INPUT)	REQUIRED LEVELS (dBm) P2 (OUTPUT)
HT/MT SIMULATION FACILITY, SATCOMA			
o UPLINK	7900-8400	-25 TO -5	-25 TO -5
o DOWNLINK	7250-7750	-40 TO -20	-40 TO -20
DSCS III COMMAND UPLINK	f_c = 8005 MHZ (KT42 OUTPUT IS S-BAND)	-40 TO -20	-40 TO -20
ALSO APPLIES TO X-BAND INTERFACE LEVELS OF AN ACTUAL HT/MT, EG. FT. DETRICK, MA			

SIMULATOR R.F. INPUT LEVEL RANGE: -40 TO -5 DBM

SIMULATOR R.F. OUTPUT LEVEL RANGE: -40 TO -5 DBM

Table 5. 700 MHZ interface levels.

MODEM TYPE	REQUIRED LEVELS	
	P_3 (DBM) INPUT	P_4 (DBM) OUTPUT
GE TEST SET	- 10 dBm	-10 TO 0 dBm
RAYTHEON PN MODEM	+ 10 dBm	-50 TO-5 dBm
OM-55, MODEM	-10 ± 3 dBm	-87 TO -27 dBm
HT/MT, DOWNLINK	0 dBm	0 dBm
HT/MT, UPLINK	0 dBm ± 10 dB	-10 TO 0
DATA EXTRACTED FROM MODEM SPECIFICATIONS AND FINAL REPORT, HT/MT		

SIMULATOR I.F. INPUT LEVEL RANGE: -15 TO +10 dBm

SIMULATOR I.F. OUTPUT LEVEL RANGE: -30 TO 0 dBm

5.2 BLOCK DIAGRAM AND FUNCTIONAL DESCRIPTION

The simulator is divided into ten functional elements as noted in the block diagram of Figure 12. A brief description of the functional blocks is given below:

a. X-Band Input Downconverter Section

This section provides a means of interfacing with the DSCS III Communications or Command Link, provides RF level control and downconversion to a 700 MHZ Intermediate Frequency (I.F.). This section uses an external synthesized source as a local oscillator. Downconverters can be added to accomodate other frequency bands.

b. I.F. Input Section

Provides a direct coaxial IF input for interfacing with modems, an actual HT/MT earth station (Eg. Fort Detrick) and witn the SATCOMA HT/MT earth station simulator. The I.F. input section permits interfacing directly with 700 MHZ modems such as the USC-28, the Raytheon PN modem and others for direct modem testing in the presence of noise, with noise and fading, and for conducting modem checkout tests prior to beginning a simulation run.

c. The I.F. Processor Section

Imposes controlled fading characteristics on input signal by means of analog modulators arranged along a densely-tapped delay line. A single tap is used for flat fading while selective fading requires multiple taps. The delay line modulators are driven by the digital controller subsystem.

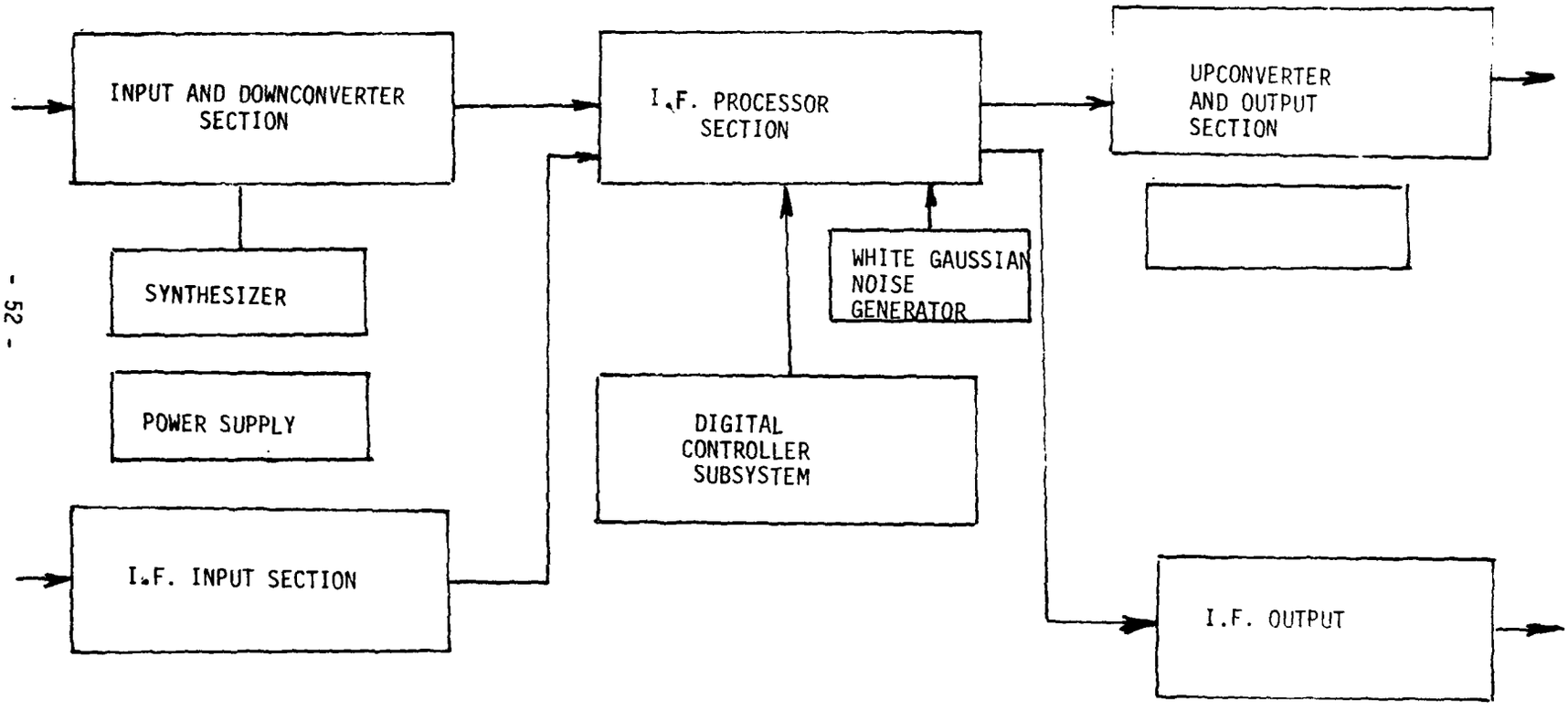


Figure 12. Functional block diagram of the fading simulator.

d. IF Output and Signal Conditioning Section

Provides a conditioned and level controlled-coaxial I.F. output at 700 MHZ $\pm$50 MHZ.

e. X-Band Output and Upconverter Section

This section provides a means of interfacing with the DSCS III Communications or Command link, provides RF level control and upconversion from 700 MHZ to that X-Band uplink or downlink frequencies.

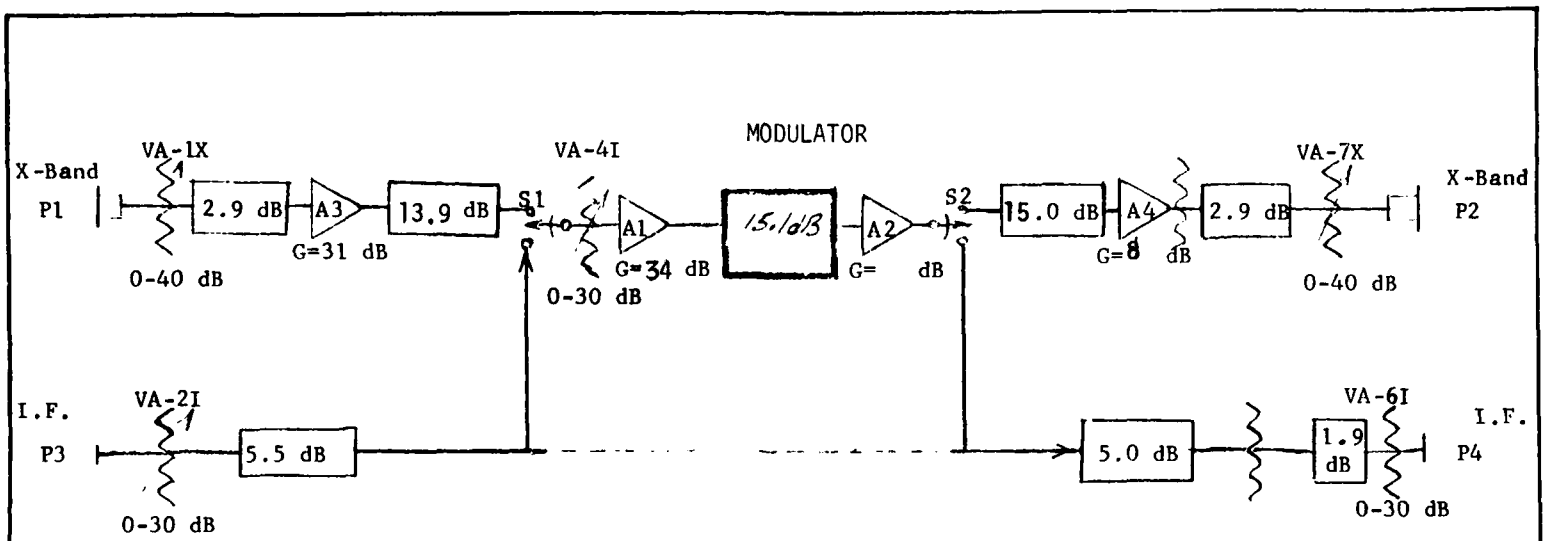
5.3 R.F./I.F. SUBSYSTEM DESIGN

The R.F./I.F. subsystem design provides input and output frequencies, power levels, impedances and connectors that are compatible with the DSCS III SHF command and communications simulator, earth stations of the HT/MT class and a variety of modems having a 700 MHz interface requirement.

5.3.1 Simulator Gain Distribution

Simulator gain characteristics have been developed to meet the interface requirements of paragraph 5.1 and to overcome the loss characteristics of the passive components. A summary of these gain distribution parameters is given in Figure 13 for the flat fading simulator and in Figure 14 for the selective fading simulator respectively. In each case, all losses are consolidated and the amplifier gain values are chosen to balance the interface conditions with the internal losses. In the flat fading design the drive level to the quadrature modulator is set at a nominal +7 dBm.

When this unit is expanded to accept the delay line processor, (Figure 14) the drive level to the delay line will be raised to +27 dBm nominal by adding a supplementary amplifier.

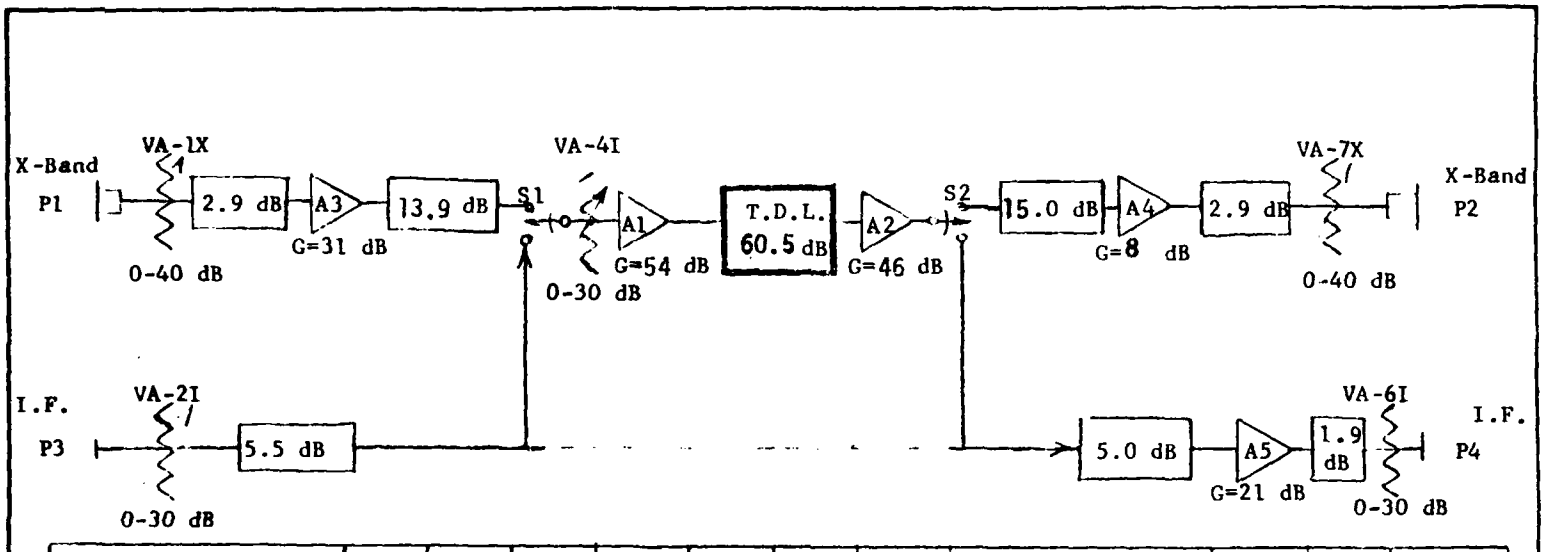


CONDITION	INPUT dBm	VA-1X Atten	A3 Input	A3 Output	VA-4I Atten	A1 Input	A1 Output	A2 Input	A2 Output	A4 Input	A4 Output	VA-7X Atten	X-Band Output
X-Band/X-Band P1/P2	-40	0	-42.9	-11.9	0	-27	+ 7	-8	+12.5	-2.5	+5.5	-40	-40 dBm
	-20	-20	-42.9	-11.9	0	-27	+ 7	-8	+12.5	-2.5	+5.5	-20	-20
	-5	-35	-42.9	-11.9	0	-27	+ 7	-8	+12.5	-2.5	+5.5	-5	-5
X-Band/700 MHz P1/P4	-40	Same as Above										VA-6I	IF Out.
	-20											-35	-30
	-5											-20	-15
												-10	-5

	Input dBm	VA-2I Atten	VA-4I Atten	A1 Input	A1 Output	A2 Input	A2 Output	A4 Input	A4 Output	VA-7X Atten	X-Band Output
700 MHz/X-Band P3/P2	-15	0	-6.5	-27	+ 7	-8	+12.5	-2.5	+5.5	0	0 dBm
	-5	10	-6.5	-27	+ 7	-8	+12.5	-2.5	+5.5	0	0
	+10	25	-6.5	-27	+ 7	-8	+12.5	-2.5	+5.5	0	0
700 MHz/700 MHz P3/P4	-15	Same as Above								VA-6I	IF Out
	-5									-30	-30 dBm
	+10									-15	-15
										- 0	0

LOSSES ARE THE MAXIMUM ENCOUNTERED

Figure 13. Simulator gain distribution, single tap case.



CONDITION	INPUT dBm	VA-1X Atten	A3 Input	A3 Output	VA-4I Atten	A1 Input	A1 Output	A2 Input	A2 Output	A4 Input	A4 Output	VA-7X Atten	X-Band Output
X-Band/X-Band P1/P2	-40	0	-42.9	-11.9	0	-27	+27	-33	+12.5	-2.5	+5.5	-40	-40 dBm
	-20	-20	-42.9	-11.9	0	-27	+27	-33	+12.5	-2.5	+5.5	-20	-20
	-5	-35	-42.9	-11.9	0	-27	+27	-33	+12.5	-2.5	+5.5	-5	-5
X-Band/700 MHz P1/P4	-40	Same as Above										VA-6I	IF Out.
	-20											-35	-30
	-5											-20	-15
												-10	-5

	Input dBm	VA-2I Atten	VA-4I Atten	A1 Input	A1 Output	A2 Input	A2 Output	A4 Input	A4 Output	VA-7X Atten	X-Band Output
700 MHz/X-Band P3/P2	-15	0	-6.5	-27	+27	-33	+12.5	-2.5	+5.5	0	0 dBm
	-5	10	-6.5	-27	+27	-33	+12.5	-2.5	+5.5	0	0
	+10	25	-6.5	-27	+27	-33	+12.5	-2.5	+5.5	0	0
700 MHz/700 MHz P3/P4	-15	Same as Above								VA-6I	IF Out
	-5									-30	-30 dBm
	+10									-15	-15
										- 0	0

LOSSES ARE THE MAXIMUM ENCOUNTERED

Figure 14. Simulator gain distribution, tapped delay line case.

5.3.2 Modulator Dynamic Range Requirements

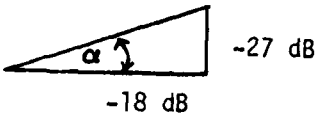
A balanced mixer having nominally a 35 dB dynamic range has been chosen for implementing the tap modulators which produce the Rayleigh fading characteristic. The 35 dB dynamic range provides greater than 99% of the Rayleigh fading range with less than 20 degrees of phase error.

Signal phase error arises because of the method used to generate the Rayleigh fading signal and the fact that a modulator is not capable of precisely attenuating signals between the lower edge of its range and infinite attenuation. If the in-phase modulating function is $x(t)$ and the quadrature function $y(t)$, where x and y have Gaussian amplitude statistics, then the recombined fading envelope $z(t)$ is

$$z(t) = x(t) + jy(t)$$

$$= R(t)e^{j\varphi(t)} \qquad (16)$$

where $R(t)$ is Rayleigh distributed and $\varphi(t)$ is uniformly distributed between 0 and π radians. When $\varphi(t) = 0$, for example, then $x(t) = R(t)$ and $y(t) = 0$. But due to leakage through the modulator, $y(t)$ may still contain a sizeable fraction of the power in $x(t)$. The effect is most severe when $R(t)$ is small (a deep fade) and the phase is a multiple of $\pi/2$ radians. For example, 98% of Rayleigh fading occurs between +8 dB above and -18 dB below the median signal. A modulator having a 35 dB dynamic range may have leakage 9 dB below -18 dB while it was nominally off. The phase error is then



$$\alpha = \tan^{-1}(10^{-9/20}) = 19.54^{o}$$

Parametric curves for this error are shown in Figure 15.

The expected region of maximum fading depth is 35 to 40 dB.

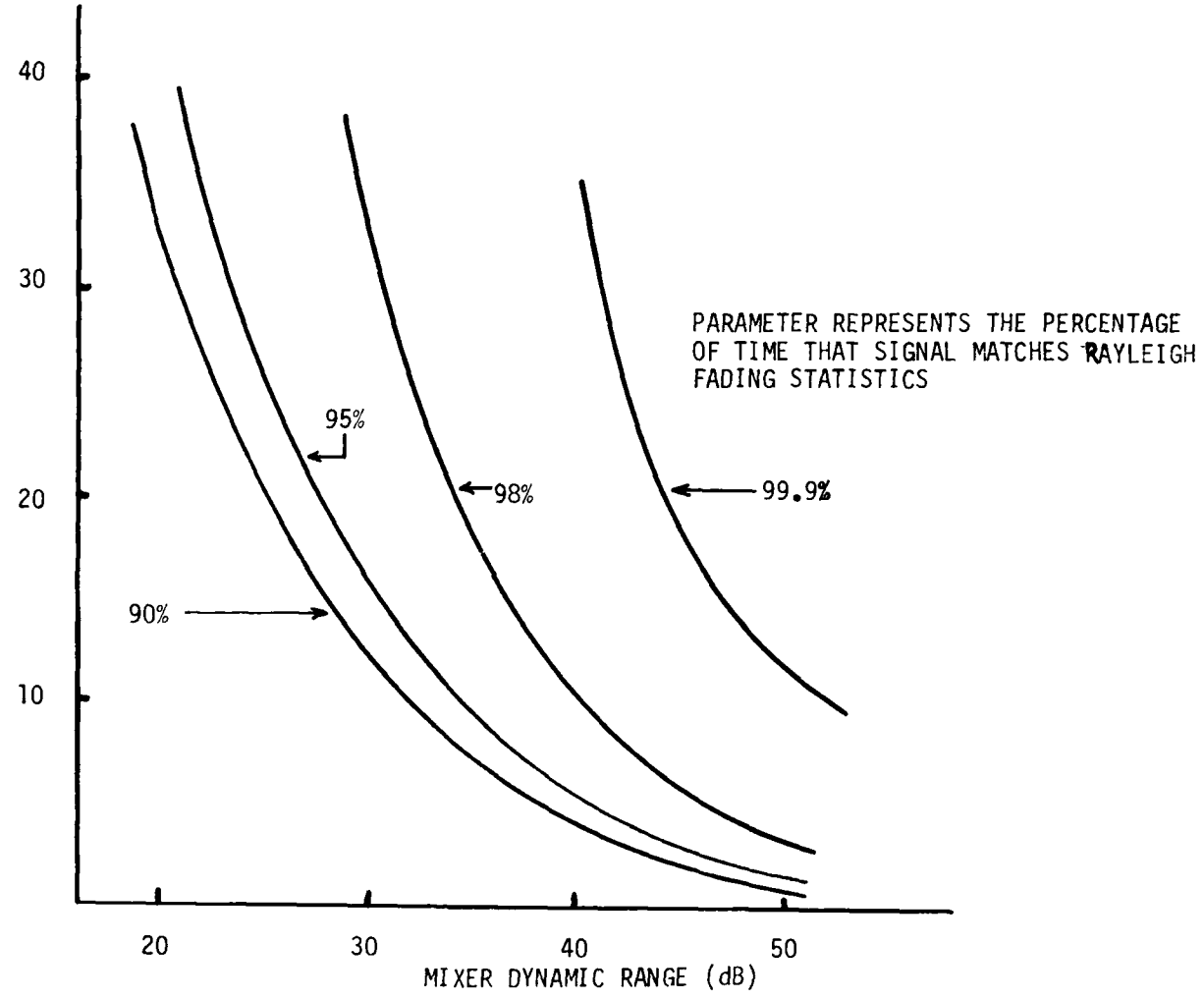


Figure 15. Error tradeoffs for tap dynamic range selection.

5.3.3 Tapped Delay Line Trades and Implementation (Selective Fading Units Only)

Coaxial cable has been selected for the delay medium for the selective fading configuration. A delay line is not required for the flat fading case. The coaxial type of delay line best satisfies the system requirements and is readily available without a development or design program. The general requirements for the line are:

Total length:	100 nsec
Taps:	50 at 2 nsec spacing
Impedance:	50 ohms input and output

The other devices considered in the tradeoff study and rejected for this application were Charge-Coupled Devices (CCD's) and Surface Acoustic Wave (SAW) devices. Figure 16 compares the general capabilities of the three delay line types studied. The CCD's cannot provide the short delays required without incurring a risk of inter-tap crosstalk because of the close physical spacing of the taps. A delay line implemented with SAW techniques will also be physically small and requires a development program.

Coaxial cable chosen for this application has a diameter of 0.141 inch, a delay of about 1.45 nsec per foot (16.5 inches per 2 nsec) and has a nominal loss of 0.1 dB per foot. The delay line design also includes the 10 dB tap couplers, which are over 1/4 wavelength in size and their SMA connectors; the result is a delay line segment of about 12.5 inches plus a directional coupler of 4 inches.

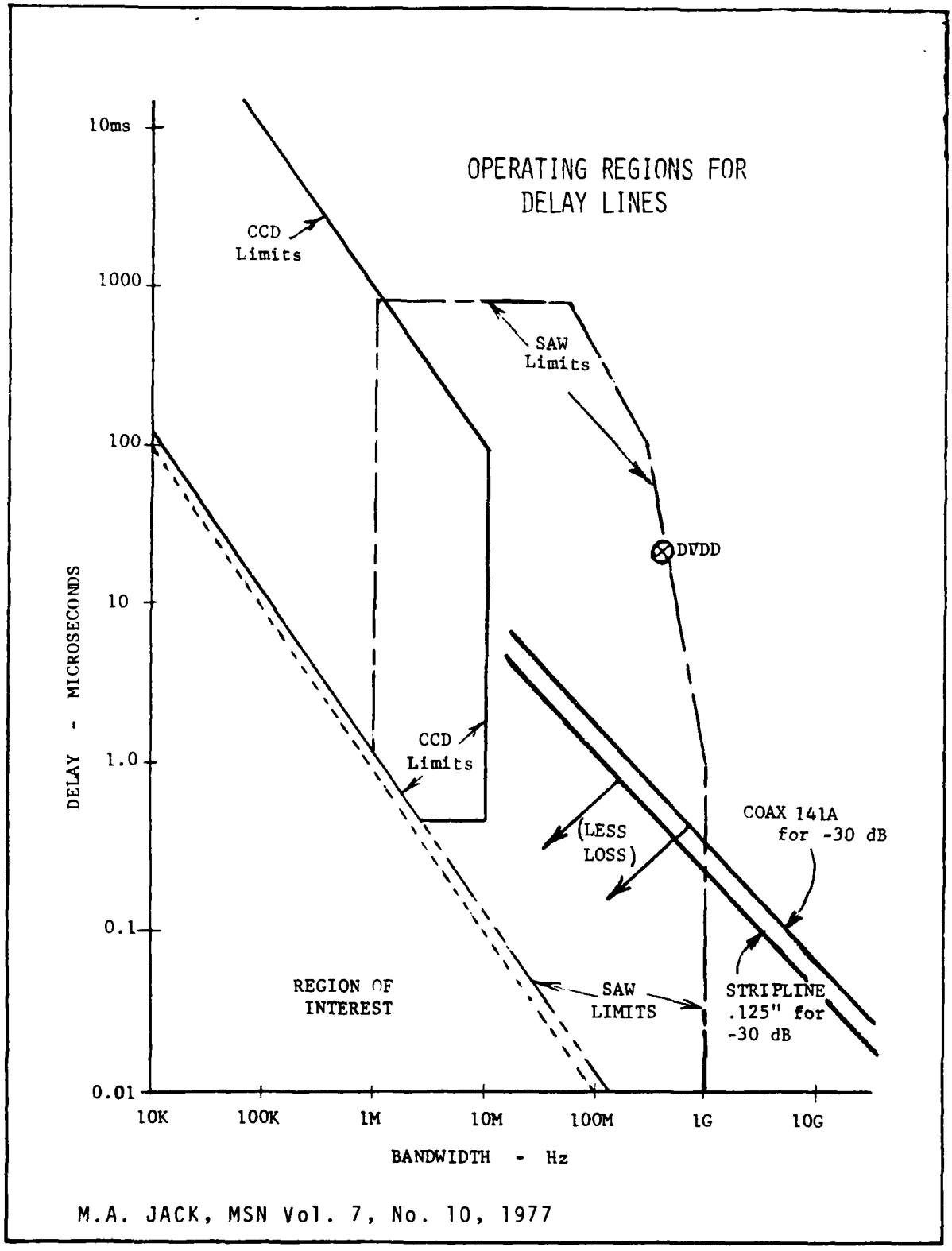


Figure 16. Coaxial cable selected for delay line implementation.

The 16.5 inches per tap will result in a total delay line length (49 segments) of 67.4 feet. The physical layout will involve a folding pattern and grounding to minimize possible crosscouplings; it also must accomodate the physical size and access requirements of the 50 modulator modules. With the connectors and the 10 dB coupler, the estimated insertion loss for each coupler (in addition to the coupling value) is 0.30 dB. The resulting outputs of the 10 couplers will then be nominally +17 dBm for the first tap and -9 dBm for the 50th tap. Actually, the first tap will have zero delay so 49 line segments are used for the 50-tap configuration with the last coupler having a 50 ohm output termination. The overall loss budget for the tapped delay line, modulator, and combining network is in Table 6.

Table 6. Tapped delay line and combiner loss budget.

ITEM		LOSS (dB) AT 50TH TAP
DELAY LINE		
Coaxial Cable		6.0
Modulator in-line insertion Losses		15.0
Power Loss due to Coupling off Energy		5.0
	Subtotal	26.0
MODULATOR		
Coupler		10.0
90^{o} Hybrid		3.3
Mixer Conversion Loss		8.5
0^{o} Hybrid		3.3
Attenuation Added to Match Required Delay Spectrum		5.0
	Subtotal	30.1
50:1 COMBINER		
Coaxial Cable		0.4
Connectors		Negligible
Combiners CB-1f CB-13		6.4
Combiner CB-18		6.4
Mismatch Loss; 0.08 dB/Junction x6 Junctions		0.5
Design Margin		0.3
	Subtotal	20.4

5.3.4 I.F. Processor Designs for Flat and Frequency Selective Rayleigh Fading

Random amplitude and phase modulation is applied to the signal under test in a quadrature multiplier. The controlling element is the time varying current delivered by the D/A converter output interfacing circuits described later in paragraph 5.4.3. This control current is applied to the in-phase (I) and quadrature (Q) mixer I.F. ports. The mixers operate as current controlled attenuators and therefore require a high value of Local Oscillator (L) port to R.F. port isolation, upwards of 35 dB or more.

The preliminary mixer selection for the flat fading modulator is the Merimac type DDM-2-500. Selection of the mixer to be used in the selective fading modulators will be accomplished in a tradeoff study conducted at a later date. These tradeoffs are to define the construction methods that will be used to implement the modulator assemblies required for the selective fading simulator units. Stripline integrated construction will be weighed against the use of conventional discrete coaxial components.

Selection of the mixers to be employed in the quadrature multipliers is based upon their L to R port isolation. The Merrimac DDM-2-500 double balanced mixer has a minimum isolation of 35 dB between L and R ports at 1 GHZ and a typical value of 50 dB in the 650 to 750 MHZ band. Output signal phase is 0^{o} or 180^{o} depending upon whether the current is positive or negative. Since the I and Q channels are independently amplitude modulated at 0^{o} or 180^{o}, the output signal vector due to their linear combination in the 0^{o} hybrid will have a uniform phase distribution. Since the combined output represents the summation

of complex samples of a Gaussian process, the output will have a Rayleigh amplitude distribution.

The requirement for a 700 MHZ dynamic operating range of nearly 40 dB (see Paragraph 5.3.2.1) places a corresponding limit on harmonic output of the mixers. To prevent harmonics of the 700 MHz IF from being propagated in the system, bandpass filtering is applied to the output of the combining network.

The modulator output signal levels must be adjusted to specific mean values in order to accurately represent the desired fading spectrum. This will be accomplished by means of an attenuator at the output of each modulator assembly. Each attenuator must be set during a calibration sequence whenever the fading scenario is changed.

The approximate range of mixer input levels and control current ranges shown in Table 7.

Table 7. Mixer input parameters.

Input Parameter	Flat Fading	Selective Fading
Available 700 MHZ input Level (dBm), Nominal	+4	+14 to -6
Control Current (mA)*	2 MA Max.	0.4 to 1 ma

*Typical - Actual range to be determined by measurement.

The actual current range will be determined by measurement, the typical data in Figure 17 illustrates the variation of attenuation range as the modulation current changes.

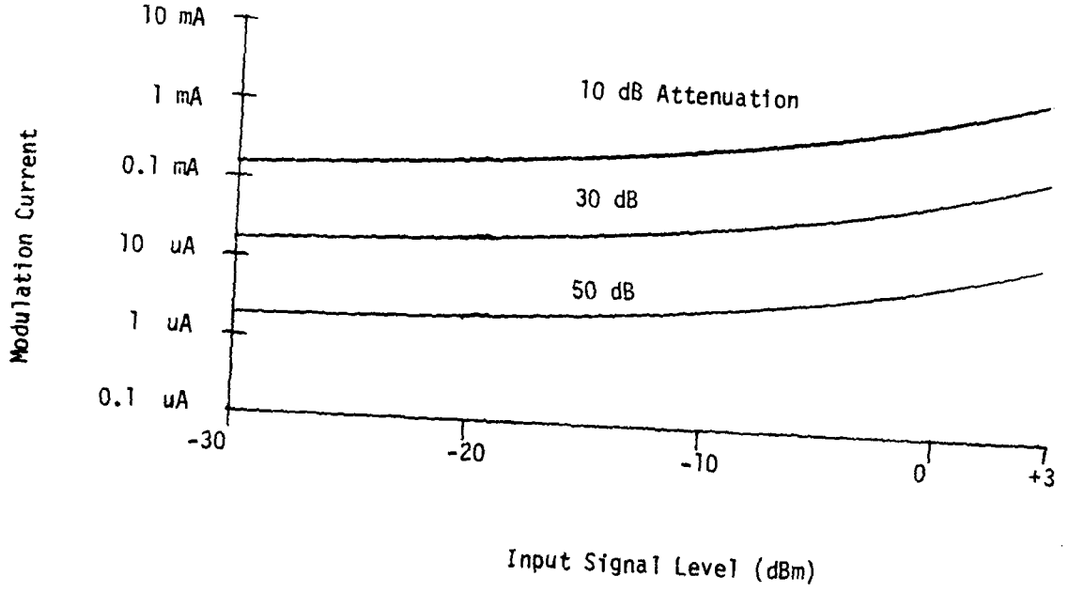


Figure 17. Modulation current required for I and Q channel attenuation.

The 50:1 combiner for the selective fading configuration will utilize commercial n-way couplers. A preliminary approach has been taken to select a group of seventeen 4-way couplers in the configuration of Figure 18.

The relationship between the major components of the IF Processor is shown in the diagram of Figure 19. The IF Processor accepts 700 MHZ inputs from the appropriate input downconverter or from the 700 MHZ input section.

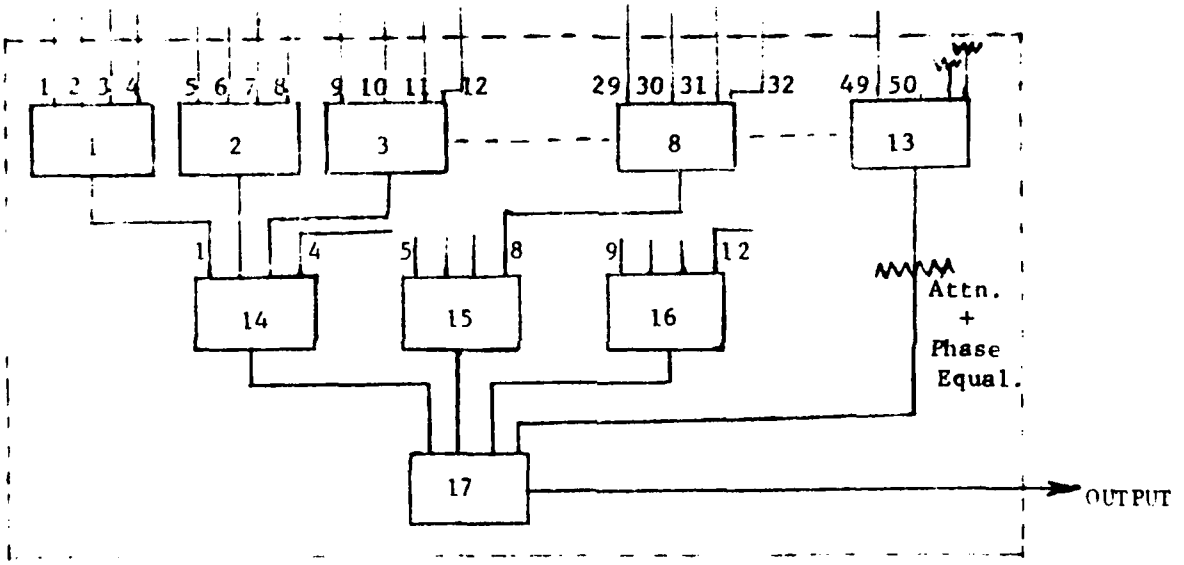


Figure 18. 50:1 combiner network.

After modulation functions are completed, the signal is bandpass filtered and amplified. An input port is available for inserting bandpass filtered white noise (see Paragraph 5.3.8). The IF processor 700 MHz output is available to either an upconverter or to an IF output port.

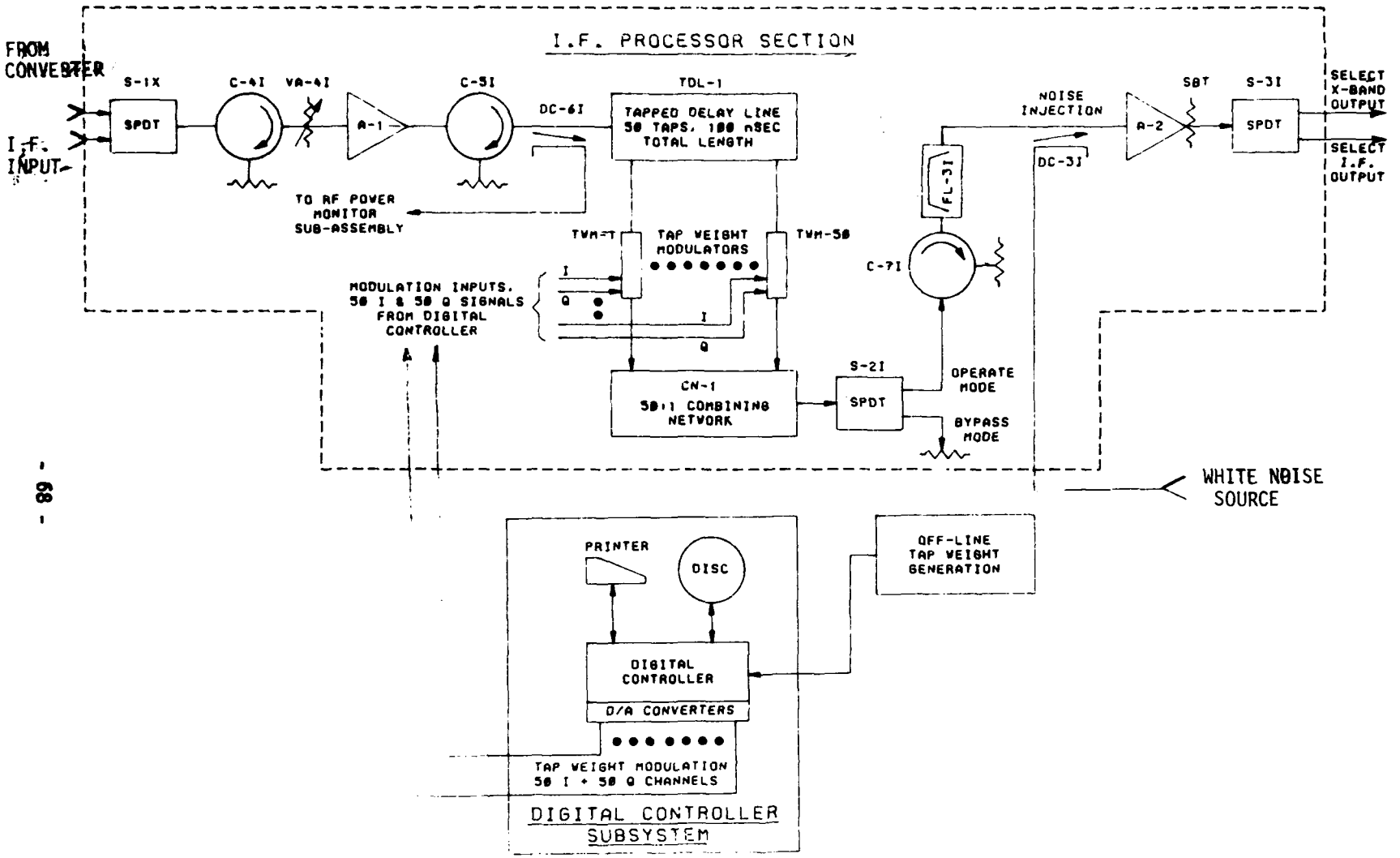


Figure 19. I.F. processor diagram.

5.3.5 Downconverter and Upconverter Design

The downconverter provides amplification, level matching and conversion of R.F. frequencies to the 700 MHz (±50 MHz) frequency of the IF Processor, Down-converters and up-converters can be added to the design at any time. Figures 20 and 21 illustrate the basic converter designs for conversion from and to X-Band respectively. A common frequency generator, an SHF synthesizer is recommended to supply the common Local Oscillator mixer injection signal. Mixer output is bandpass filtered to eliminate unwanted sidebands and thereby reduce the mixer noise figure by 3 dB. The filter FL-II is centered at 700 MHz with an operating bandwidth of 100 MHz.

In the upconverter, two post-mixer filters are required to provide operation over the DSCS III 500 MHz uplink and the 500 MHz downlink bands, which are separated by 150 MHz. Separate filters are required to assure rejection of the undesired mixer sidebands. Uplink/downlink filter selection will be by means of coaxial switches.

Accomodation of all DSCS-III channels requires the local oscillator injection frequencies shown in the Frequency plan described in Table 8. The injection frequency is common to both the X-Band up and downconverters. Since the frequencies have been chosen to prevent spectrum inversion in both converters, any combination of X-Band input/output or IF input/output connectivity can be accomodated. The same design strategy can be applied to other conversion bands as needed during the lifetime of the fading simulator.

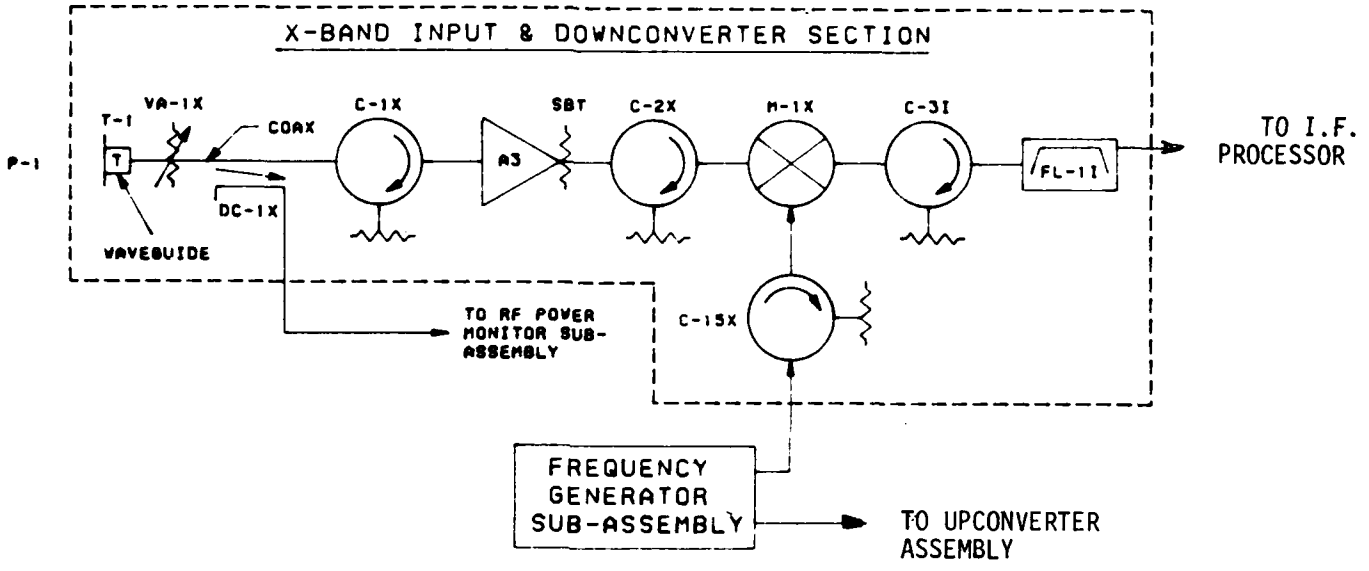


Figure 20. X-band input and downconverter assembly.

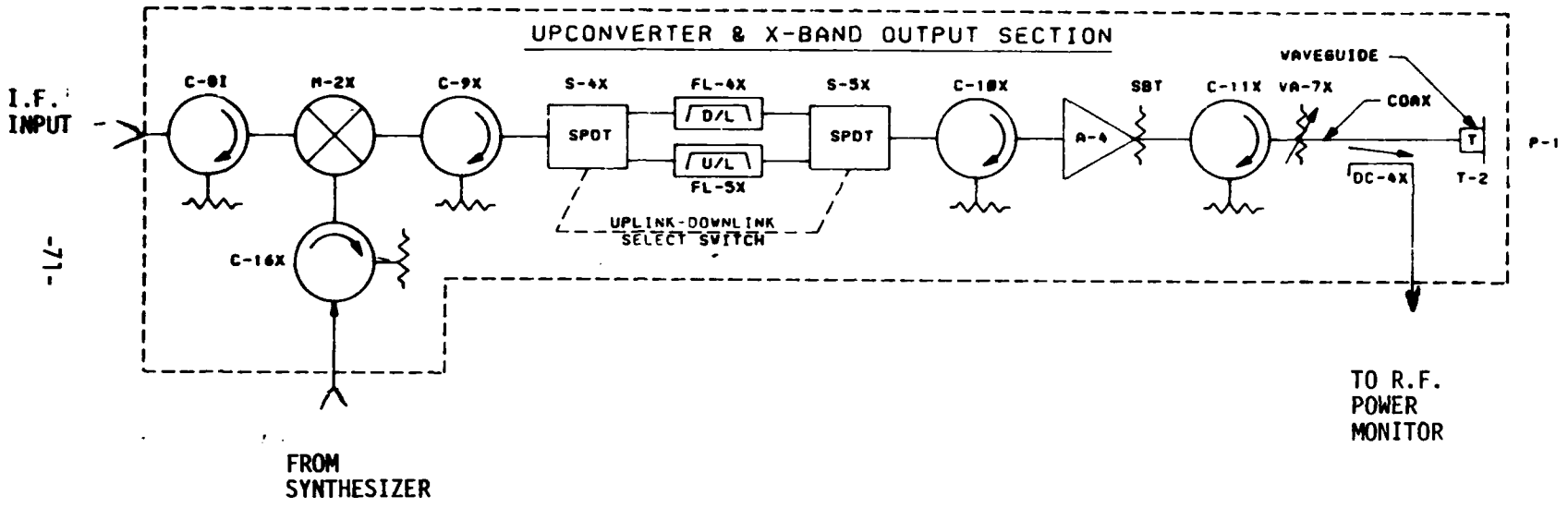


Figure 21. Upconverter and X-band output section.

Table 8. Frequency plan.

UPLINK SIMULATION					DOWNLINK SIMULATION		
DSCS III CHANNEL	UPLINK BAND (MHz)		BANDWIDTH (MHZ)	SIMULATOR LOCAL OSCILLATOR FREQUENCY (MHZ)	TRANSMIT (MHZ)		SIMULATOR LOCAL OSCILLATOR FREQUENCY (MHZ)
	f_L	f_H			f_L	f_H	
1 & CMD-1	7975	8035	60	7305	7250	7310	6580
2	8060	8120	60	7390	7335	7395	6665
3	8145	8230	85	7487.5	7420	7505	6762.5
4	8255	8315	60	7585	7530	7590	6860
5 & CMD-2	8340	8400	60	7670	7615	7675	6945
6	7900	7950	50	7225	7700	7750	7025

UPLINK: 7900-8400 MHZ
DOWNLINK: 7250-7750 MHZ
SIMULATOR IF: 700 MHZ

Frequency accuracy is an important parameter when testing with the Raytheon Pseudo-Noise (P.N.) modem. This modem requires a frequency accuracy of $\pm$3500 Hz at the 700 MHz center frequency, corresponding to 5×10^{-6}. The propagation simulator frequency accuracy must be at least 4×10^{-6}, as shown in Table 9.

Table 9. Frequency accuracy budget.

MODEM FREQUENCY ACCURACY REQUIREMENT		5×10^{-6}
DSCS III PAYLOAD ACCURACY		1×10^{-6} (WITHIN 4 HOURS AFTER TURN-ON)
ACCURACY REQUIRED FOR PROPAGATION SIMULATOR	=	4×10^{-6} AT 700 MHZ

5.3.6 Filter Requirements

Broadband filtering of band-pass signals is used to constrain the maximum simulator effective noise bandwidth to 1.3 times that of an ideal rectangular filter and to suppress the unwanted sidebands of the downconverter and the upconverter. This bandwidth is sufficiently broad to produce only a minor increase in the deviation from linear phase as compared to an unfiltered systems and therefore has a negligible effect on the bit error rate. The output of the additive white Gaussian noise (AWGN) source is filtered to constrain the noise spectrum to about 100 MHZ. Nominal filter specifications are given in Table 10.

Table 10. Summary of filter specifications.

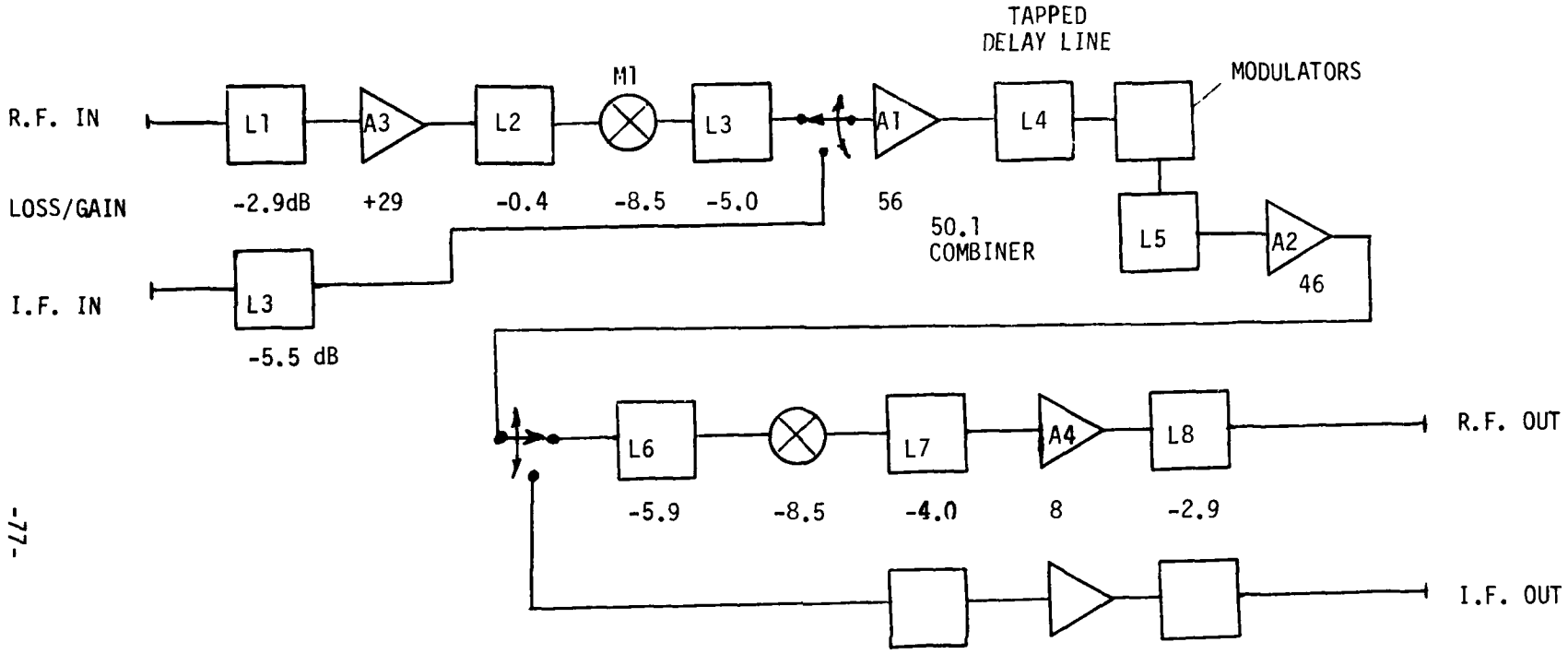
PARAMETER	I.F. FILTERS
CENTER FREQUENCY (MHZ)	700
BANDWIDTH (MHZ) TO 1dB ROLLOFF	100
REJECTION BAND (MHZ)	30 dB AT 600, 800
INSERTION LOSS OVER PASSBAND (dB)	1.0
PASSBAND INSERTION LOSS VARIATION (dB)	0.1
RETURN LOSS,MINIMUM (dB) IN PASSBAND	15
GROUP DELAY VARIATION (NANOSECONDS)	10

5.3.7 Noise Figure Analysis

Valid communications testing can only be accomplished when the internally-generated thermal noise of the test set has a negligible additive effect on the signal-to-noise (S/N) ratio or on the equivalent energy per bit-to-noise density ratio, E_b/N_0. A worst-case noise figure analysis has been accomplished to insure that this condition will be met for both the flat fading and the selective fading cases. In both cases, a 35 dB fade is assumed. In the selective fading case, the worst-case analysis is based upon a distribution of mean signal power defined by Figure 10 and simultaneous 35 dB fades at each of the 50 taps. The likelihood of simultaneous 35 dB fades at each of the 50 taps is infinitesimally small because the time sequence of the fading depth at adjacent taps is only weakly correlated.

The noise figure for the simulator is determined from the model shown in Figure 22. The model shows the loss, gain, and noise figure parameters used in the analysis. The output of the model includes both the overall noise performance and the specific performance at the last top of the delay line with a 35 dB fading range; the maximum expected level is 8 dB above the median value and the minimum expected level is 27 dB below the median value. Calculated Noise Figures are given in Table 11.

The output S/N ratio of the flat fading simulator is substantially above the operational needs of known modems, even at fading ranges of 35 dB.



$$F_1 = 10 \text{ Log } \left(\frac{T_{eff}}{290} - 1 \right)$$

$$T_{eff} = \sum_{i=1}^{n} T_i$$

$$T_i = \frac{L_1, L_2 \ldots\ldots\ldots\ldots L_i\text{-}1 \ (L_i - 1)}{G_1 \ G_2 \ldots\ldots\ldots\ldots G_i - 2}$$

For Active Components, Substitute $(f_i - 1)$ for $(L_i - 1)$

Figure 22. System noise model.

Table 11. Simulator noise figure and output S/N ratio, flat fading case.

INPUT PORT	NOISE FIGURE (dB)		INPUT POWER (dBm)	OUTPUT S/N RATIO (dB)	
	MINIMUM FADE*	35 dB FADE		MINIMUM FADE*	35 dB FADE
R. F.	6.6	25.0	-40	46.3	27.9
I.F.	11.7	42.6	-15	66.2	35.3

* CORRESPONDS TO 1% OF TIME (+8 dB RELATIVE TO THE RAYLEIGH MEDIAN VALUE)

5.3.8 White Noise Injection

A white Gaussian Noise source with amplification and level control is used as a means of adjusting E_b/N_0 at the simulator output. The circuit shown in Figure 23 consists of a noise diode followed by an amplifier and bandpass filter to confine the noise to the 650 to 750 MHz I.F. band. A variable attenuator provides a level adjustment, and the signal is coupled into the simulator at a low signal level point.

A noise diode has been selected to provide an excess noise ratio (ENR) of 35 dB. Its output noise power over a 100 MHz bandwidth is -59 dBm in the 700 MHz region. The power required for a 0 dB S/N at amplifier A2 input is -33.8 dBm, the total gain required is then 37.2 dB which covers circuit losses of 2 dB and the directional coupler value of 10 dB. The circuit also includes an attenuator for level control and a bandpass filter to limit the noise bandwidth.

We have made a preliminary selection of the Microwave Semiconductor Corp. Model MC-100 noise source. For the noise amplifier, the Watkins Johnson Model MC-1000 6203-336 has been selected. Other preliminary selections of components include the following:

- Variable Attenuator — Merrimac model AU-46AN
- Bandpass Filter — MDL model TBD
- 10 dB Directional Coupler — Anaren model 10014-10

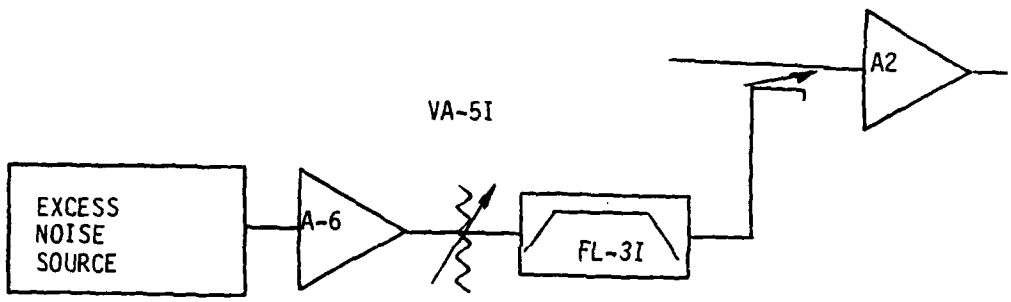


Figure 23. White noise injection circuit.

The selective fading simulator incorporates the delay line and therefore has higher internal losses, resulting in a higher simulator noise figure. A summary of the noise figure and output S/N ratio characteristics of the selective fading simulator appears in Table 12. These results are based on the delay density spectrum of Figure 10.

Table 12. Simulator noise figure and output S/N ratio, selective fading case.

INPUT PORT & FADE DEPTH	NOISE FIGURE (dB)		INPUT POWER (dBm)	OUTPUT S/N RATIO (dB)	
	OVERALL SIMULATOR	AT 50TH TAP ONLY		OVERALL SIMULATOR(1)	AT 50TH TAP ONLY
R.F.					
NO FADE(2)	7.0	12.7	-40	45.9	40.2
35 dB FADE(3)	31.5	46.5	-40	21.4	6.4
I.F.					
NO FADE(2)	15.5	29.3	-15	62.4	48.6
35 dB FADE(3)	49.2	64.2	-15	28.7	13.7

(1) INCLUDES NOISE CONTRIBUTIONS FROM ALL 50 TAPS. (2) +8 dB RELATIVE TO RAYLEIGH MEDIAN.
(3) SIMULTANEOUS FADE AT EACH OF THE 50 TAPS

The output S/N ratio of the selective fading simulator exceeds the operational needs of known modems. Under operational conditions, with independent fading, the effect of simulator-generated thermal noise will have a non-measureable effect on bit error rate.

5.4 Digital Controller Subsystem Design

The principal function of the Digital Controller Subsystem is to read data from a mass storage device and write the data to a bank of Digital to Analog (D/A) converters, at a controllable real-time rate. Each D/A converter has a filtered output which is a tap modulating function for one of the I and Q modulators at each of the 50 taps of the tapped delay line. Data may be transferred from a central location to the simulator site by means of a flexible disk. Figure 24 is a functional description of the digital controller subsystem.

Design of the digital controller is based upon the need for the unit to be expanded from the initial implementation of a single tap (flat fading) modulating function to the final version capable of providing the 50 tap (selective fading) modulating function, as described in paragraph 5.5.

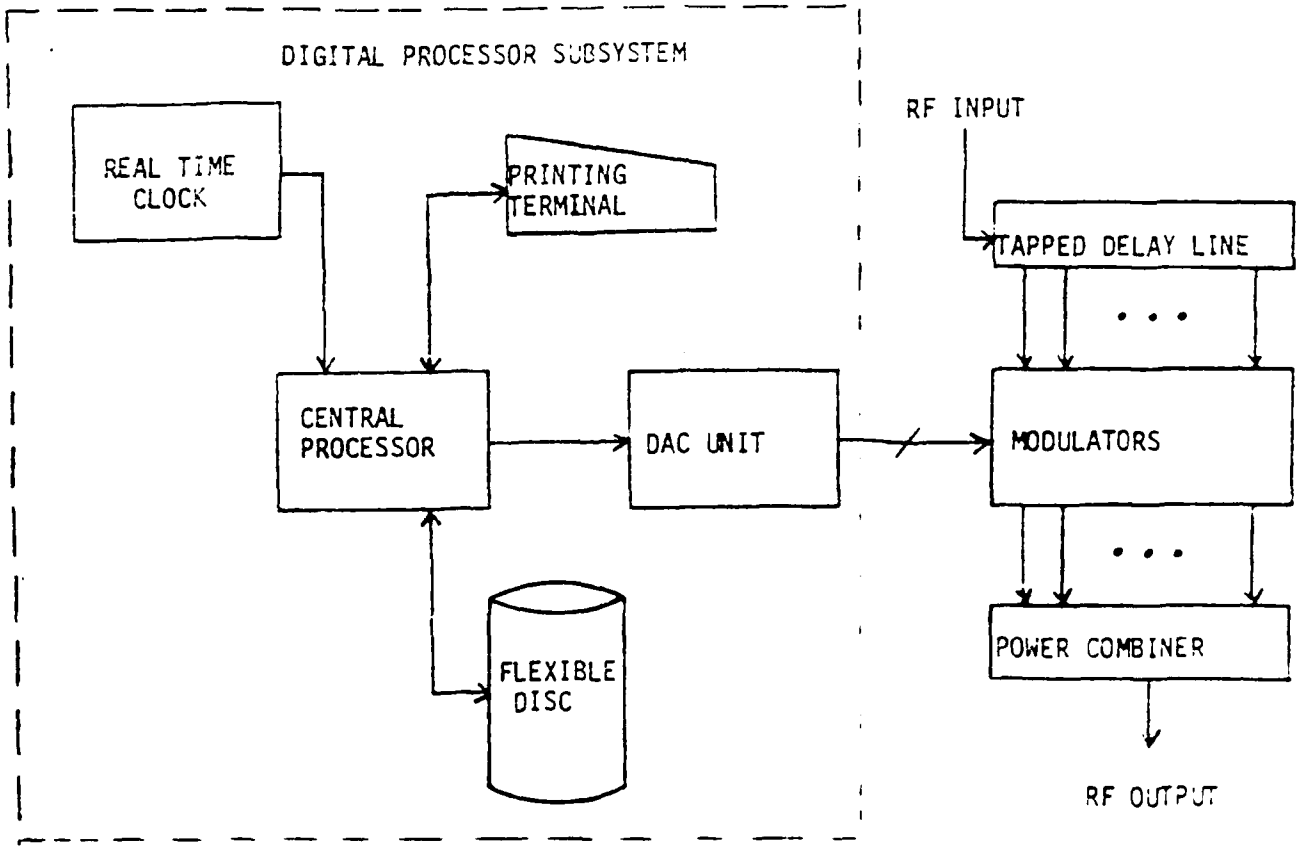


Figure 24. Functional block diagram of the digital controller subsystem.

5.4.1 Digital Controller Requirements

The digital controller requirements are structured in a manner that provides an orderly transition from the flat fading to the frequency selective fading design. The central processor has been sized to handle the memory addressing and speed requirements of the more demanding selective fading simulation. Characteristics of the digital controller subsystem for the flat fading simulator include:

- CPU with 64 kilobytes memory
- Controllable D/A Converter update rate with peak modulation rate of two kilobytes/second/modulator
- Flexible disc drive for data and program entry
- Fortran and assembly language for program development (first unit only)
- Rack-mounted components

The digital controller for the selective fading simulator will be required to drive up to 100 D/A converters at a peak of two kilobytes/second for a total memory transfer rate of 200 kilobytes/second. The memory size requirement for decorrelation times (τ_o) above about 5 ms is determined by

$$\text{Memory Size} = (200\ \tau_o) \times \left(\frac{10}{\tau_o}\right) \times (100)$$
$$= 200{,}000 \text{ bytes},$$

Where 200 τ_o is the desired test time in seconds, $10/\tau_o$ is the D/A Converter rate (bytes/sec), and 100 is the number of modulators. Below τ_o = 5 ms, the sampling rate is held at 2 KHz (see Appendix III).

5.4.2 Architectural Trades

Two main parameters of the simulated fading task drive the proposed digital controller architecture. They are the fading frequency which sets the memory transfer rate and the experiment duration which defines the memory size. Paragraph 5.4.1 defined the process which has lead to a processor design goal of 200K transfers/second and the 200K byte memory size. Five processors were selected for initial comparison. Comparison factors were primarily speed-related although direct addressing capability was also included. Results of this comparison are tabulated in Table 13.

Although the upper memory transfer rate is difficult to accurately predict since it is highly influenced by the actual program utilized, it is clear that the Intel SBC 86/12 is more closely matched to the speed requirement than any of the other candidates.

Particular advantages are that the Intel MULTIBUS scheme is well documented and that General Electric has design experience with bus-compatible cards. The D/A converters will be addressed as memory located on the same bus as the processor for optimum throughput. The program memory resides on a local bus on the processor card which allows the processor program to run while the MULTIBUS is used for DMA transfers between memory and D/A converters. This is a significant advantage over other candidate processors.

The proposed processor utilizes a twenty bit address bus, allowing direct addressing of one megabyte of memory. Organization of the proposed digital controller will be on the basis of 64 Kbyte segments. One segment may be used for the local program memory on the processor card. Four segments would be used for the data base which will reside in four memory cards and one segment will be used for the D/A converters. Ten segments would be available as spare capability for expansion. None of the other candidate processors have this equivalent expansion capability.

Timebase for scheduling data transfers to allow for variable fading frequency is located on the processor card. Other candidate systems would require auxiliary time base cards. The same is true for the operator console RS232 serial interface.

Packaging of D/A converters in a single, bus-linked chassis proved to be a problem with any candidate system. A bus extender has been chosen to meet the maximum throughput requirements. Although a bus extender will result in some unavoidable speed penalty, it should be less with a custom General Electric design than with a manufacturer's general purpose product. The excellent documentation of the Intel MULTIBUS over other candidates makes this a viable approach.

Table 13. Speed comparison of candidate processors.

PROCESSOR	MACHINE CLOCK	INDEXED MEMORY READ/WRITE	MAXIMUM DMA SPEED	DMA TECHNIQUE
INTEL SBC 80/20	2 MHZ	3.5 μS	1M BYTE/SEC/330K BYTES/SEC	BUS LOCK/BUS SHARING
INTEL SBC 86/12	(8 MHZ)	(1.8 μS)	1 M BYTE/SEC/330K BYTES/SEC	BUS LOCK/BUS SHARING
DEC PDP 11/04	3.3 MHZ	9.3 μS		BUS SHARING
DEC PDP 11/35		4.5 μS		BUS SHARING
HP 2109 EK	6 MHZ	3.8 μS	1.8 M BYTE/SEC.	CYCLE STEAL

5.4.3 Selection of the Digital-to-Analog (D/A) Converters

For the intended application, the D/A Converters must have an output current (or voltage) characteristic that matches the modulator mixer attenuation versus current characteristic, except for a gain constant. Ideally, the composite attenuation characteristic of the D/A Converter and the modulator (mixer) should be linear in dB so that quantization and scaling errors are distributed in proportion to the degree of attenuation required. Since the mixer attenuation characteristic is logarithmic, a logarithmic D/A converter is needed. Additionally, one bit must be dedicated as a sign bit and sufficient resolution must be attained with the remaining bits in a D/A converter whose bit structure is directly compatible with the byte structure of the candidate processors. Achievement of these requirements is attainable with 8-bit companding (compression/expansion) D/A converters employed for speech processing in digital telephony application. The Precision Monolithic Model DAC-76 has been chosen as the leading candidate for this application. Preliminary interface circuits have been derived and are discussed in Paragraph 5.4.4.

The DAC-76 D/A converter provides the dynamic range of a sign + 12 Bit linear D/A converter in a sign + 7 Bit format. The tranfer function is implemented by using three bits to select one of eigh binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. Accuracy is assured by specifying chord end-point values, chord nonlinearity, and monotonicity over the full operating temperature range.

The output of the DAC-76 is an approximation to the -255 law which can be expressed as:

$Y = 0.18 \ln (1 + \mu x)$ where:

X = Normalized input signal level of the compressor (encoder), V_{IN}/V_{FS} with values from -1 to +1.

Y = Output signal level of the encoder

$\mu = 255$

This law is implemented by the DAC-76 with an eight chord (or segment piecewise linear approximation for each polarity with sixteen linear steps in each chord. The D/A Transfer function is shown in Figure 25.

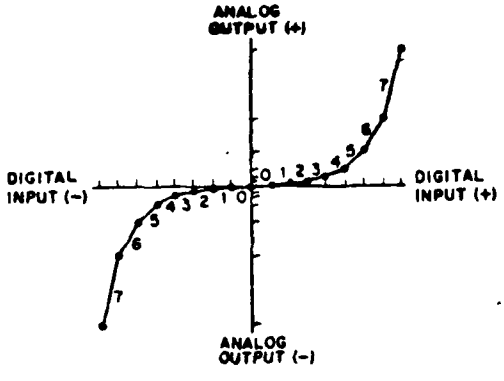


Figure 25. D/A transfer function response is logarithmic.

Table 14 relates step size in each chord to other commonly encountered measurements and to the equivalent, conventional, bindary-coded D/A converter, Step size (except in Chord 0) is about 0.3 dB and is a 1 1/2 step change between the maximum code in each chord and the minimum code in the next chord to smooth the chord transitions.

A composite response of the D/A converter and the mixer is derived in Figure 26 a, b, c. The normalized mixer attenuation characteristic is described in Figure 26a, with the mixer current normalized to the linear range. 1.0 mA on this figure corresponds to 3 mA of current. A maximum upper range is approximately 10 mA and the survival range of most mixers is about 50 MA. The D/A converter and the interface circuits are designed for a nominal 10 dB margin about the typical mixer characteristics to accomodate tolerances between mixers.

The D/A converter output current characteristic has been normalized and plotted against the specific chord end points in Figure 26b. Combining the attenuation versus required mixer current values of Figure 26a with the D/A converter output current versus chord (corresponding to digital words) results in the desired decibel linearization in the composite response of Figure 26c.

Table 14. Step size summary table.

DECODE OUTPUT (SIGN BIT EXCLUDED)

CHORD	STEP SIZE NORMALIZED TO FULL SCALE	STEP SIZE IN μA WITH 2007.75μA FULL SCALE		STEP SIZE IN DB AT CHORD END POINTS
		NORMALIZED	NUMERIC	
0	2	0.0078	0.5	0.6
1	4	0.0156	1.0	0.38
2	8	0.031	2.0	0.32
3	16	0.0625	4.0	0.31
4	32	0.125	8.0	0.29
5	54	0.25	16.0	0.28
6	128	0.5	32.0	0.28
7	256	1.0	64.0	0.28

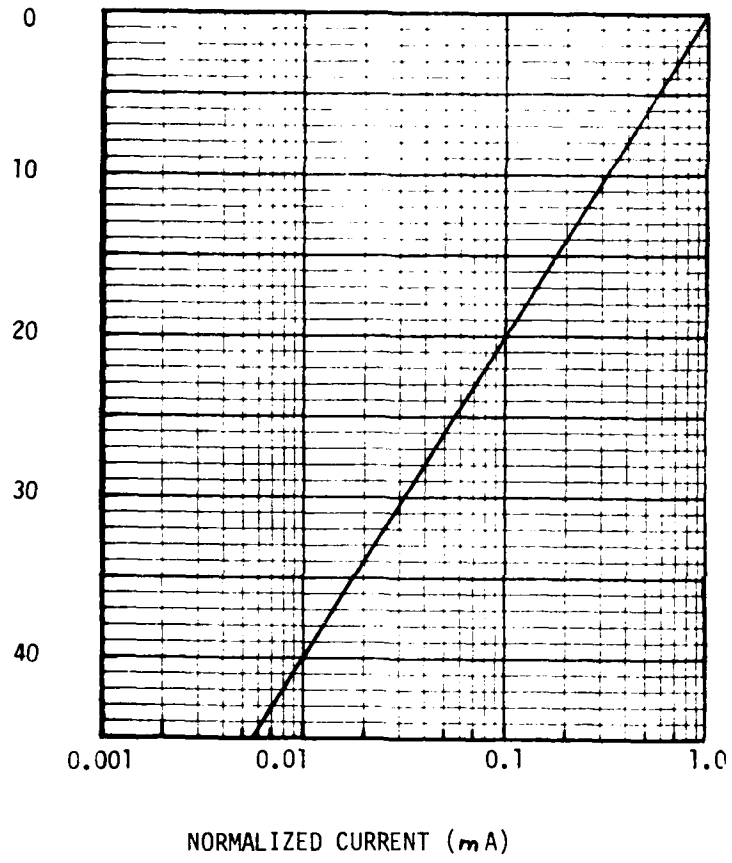


Figure 26a. Mixer attenuation characteristic (normalized).

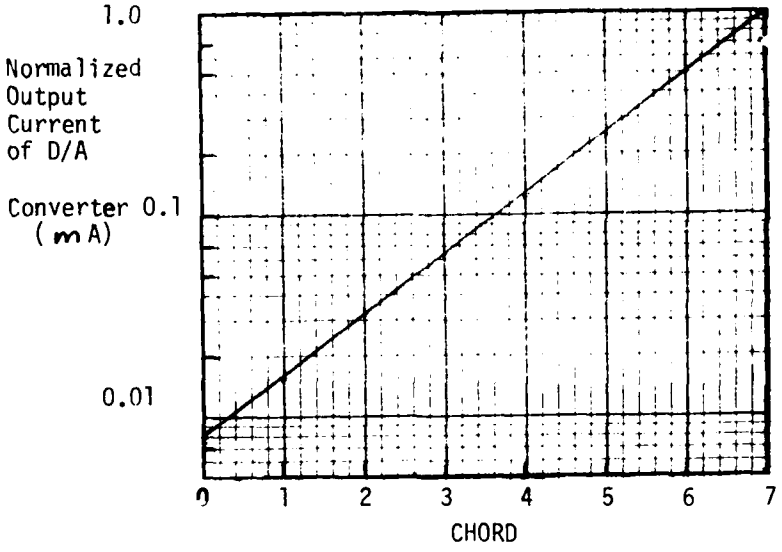


Figure 26b. D/A converter transfer characteristic.

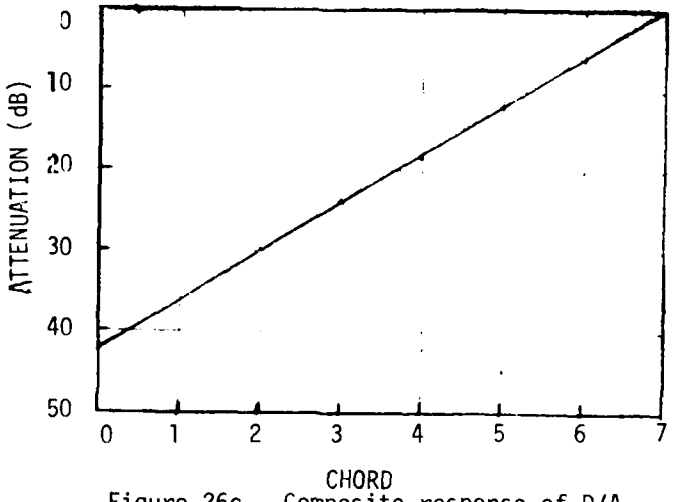


Figure 26c. Composite response of D/A converter and mixer attenuation characteristic is linear in dB.

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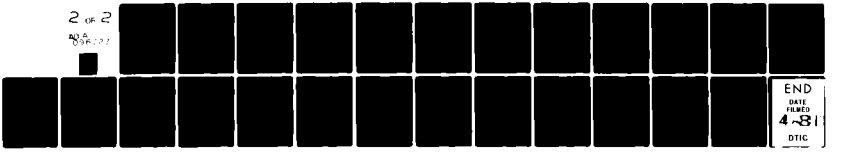

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5.4.4 Digital Controller Interfaces

The interface between the digital controller and each of the tap weight modulators will be accomplished by means of a D/A converter, an analog low pass filter and a current driver. There will be one D/A converter and interface circuit for each current controlled attenuator (mixed) in the tap weight modulators. Flat fading units will therefore contain two D/A converters and the selective fading units will contain one hundred D/A converters and their associated circuitry. Since the case of 100 D/A Converters is the most complex and the initial flat fading design must be capable of being upgraded to the selective fading case, all software and hardware definition addresses the more complex case at the outset.

5.4.4.1 I.F. Processor and D/A Converter Interfaces - One hundred digital-to-analog converters will convert digital data bytes to attenuation control currents in the IF processor for the one hundred tap modulators. The candidate D/A Converter and its performance criteria are described in Section 5.4.3. A definition of the Digital Controller interfaces is given in Figure 27. Descriptions of the D/A Converter Interfaces follow in this paragraph and the peripherals interfaces are treated in paragraph 5.4.4.2.

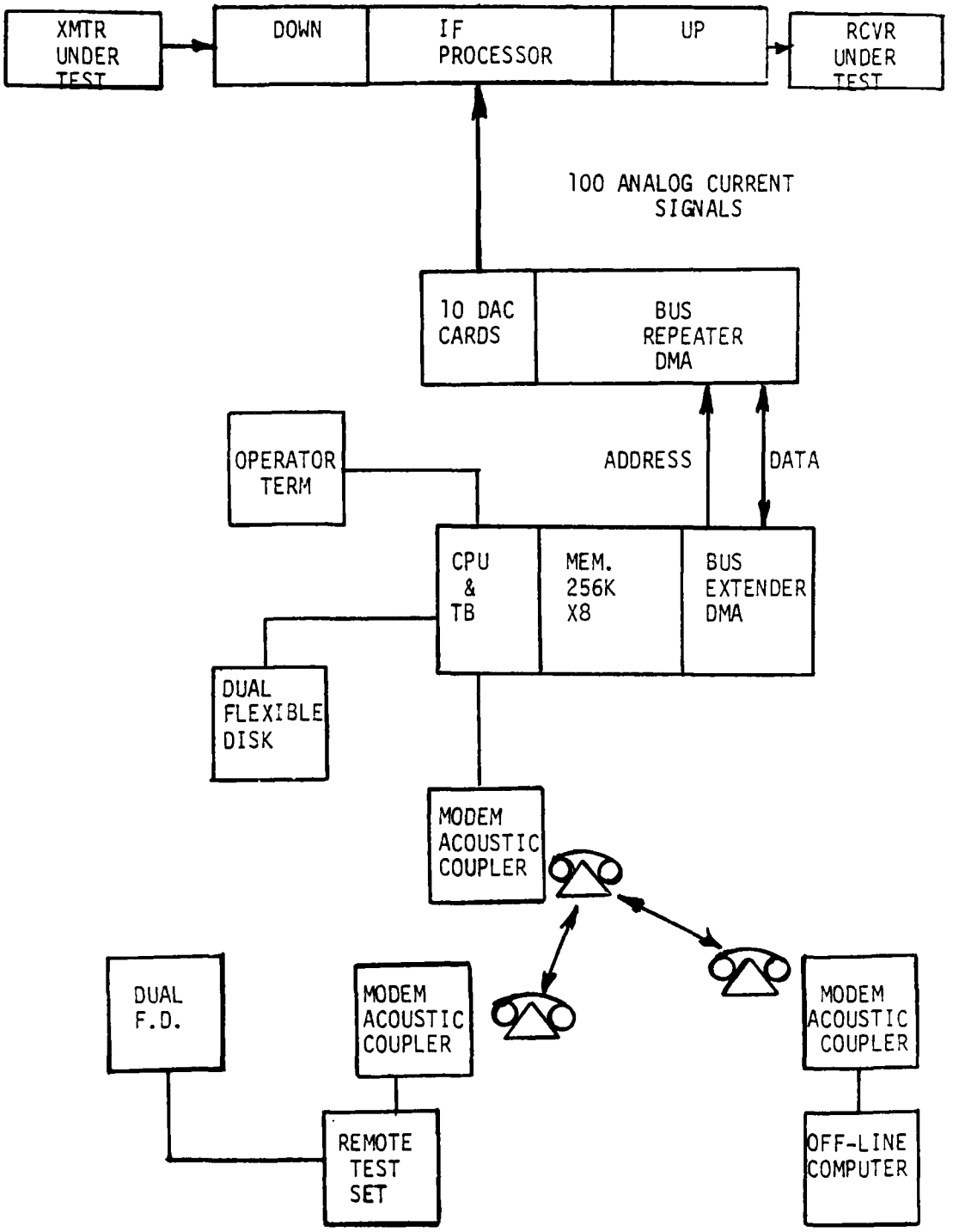


Figure 27. Digital controller interfaces.

The D/A converters, analog low-pass filters, and current mode modulator drive circuits shown in Figure 28 are organized eight to a circuit board with common address decode, bus buffers and voltage reference circuitry. Addresses shall be bank selected by a DIP switch such that a single card design may be used interchangeable with a minimum of adjustment. D/A Converter cards will be of a double-sided printed circuit construction although the first model will be wirewrap construction to prove the design. Analog circuits will use bipolar twelve volt power. The method of organizing the circuit boards in the INTEL chassis is defined in Figure 29.

D/A converter Cards will interface to the microprocessor bus using the Intel MULTIBUS definition. Actual bus signal utilization and address decoding will not be determined until the detailed design is completed. D/A converter boards will present unit load to the bus and D/A converter backplanes shall be commercially available modular MULTIBUS units of double-sided Printed Circuit Board construction.

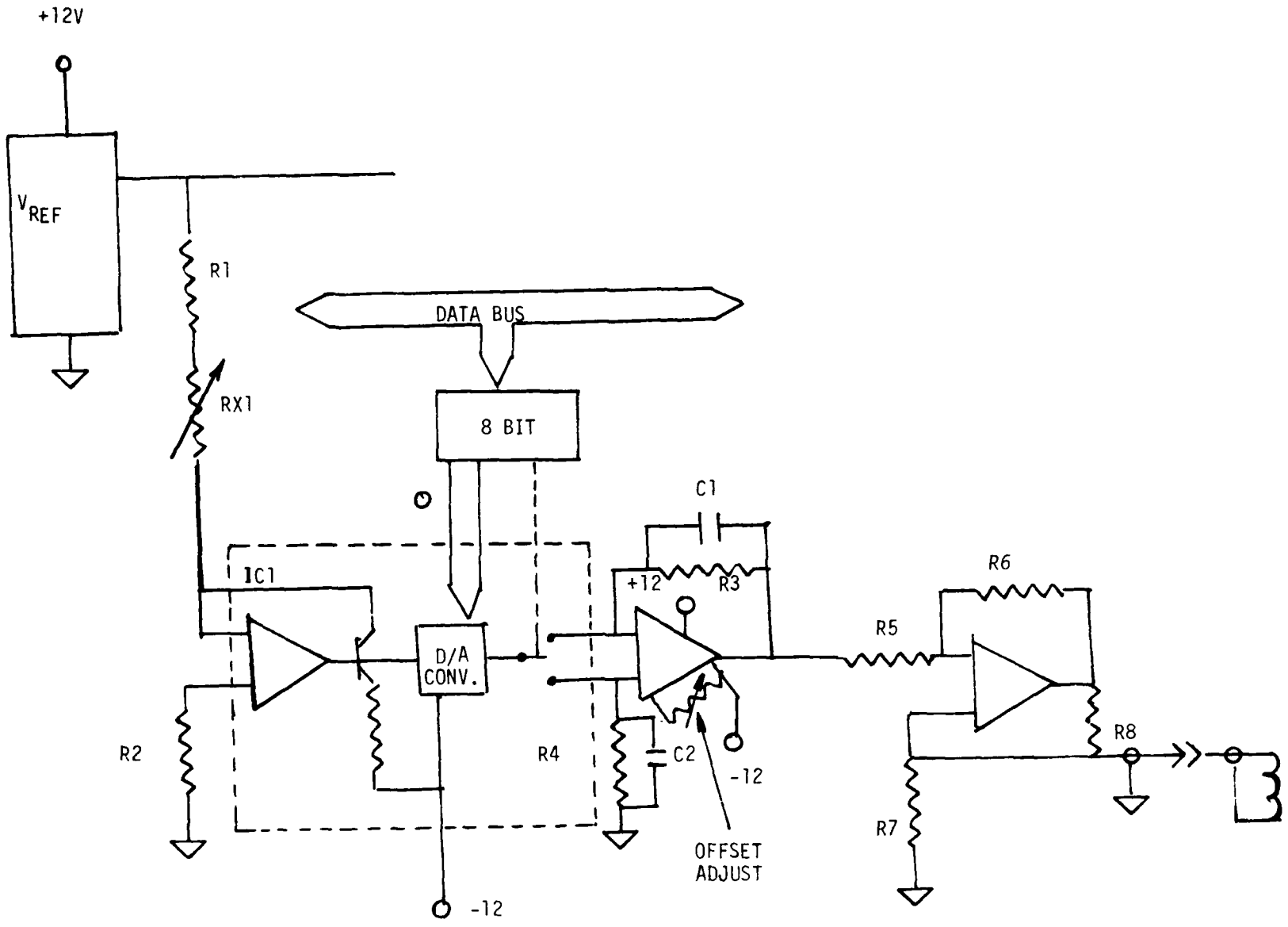


Figure 28. Interface between microprocessor and quadrature modulators.

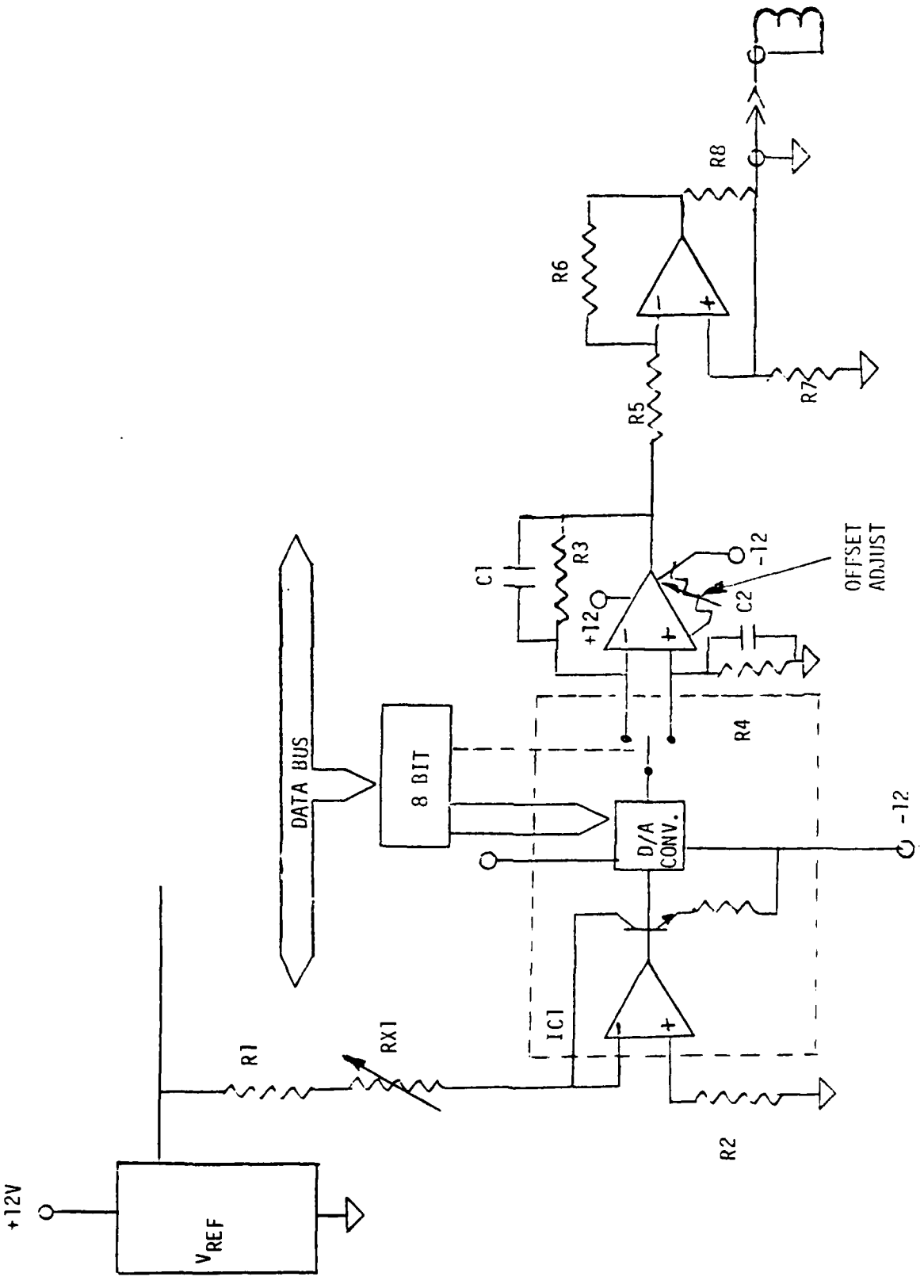
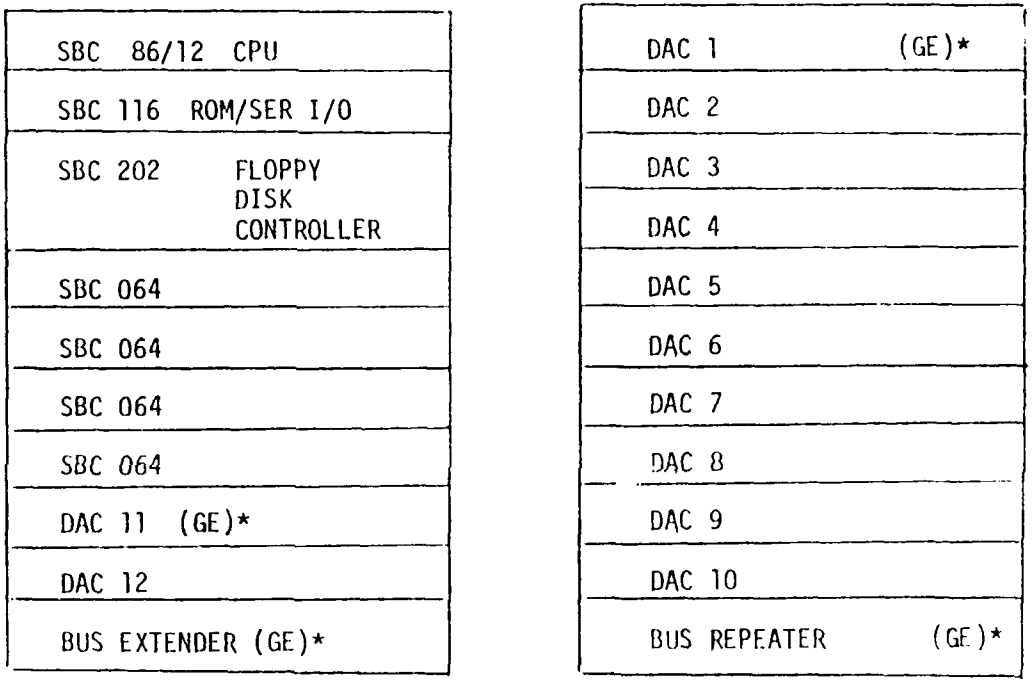


Figure 28. Interface between microprocessor and quadrature modulators.



* INDICATES DESIGN AND CONSTRUCTION BY THE GENERAL ELECTRIC CO.

Figure 29. Board organization of the digital controller.

The Digital to Analog (D/A) Converters chosen for this application provide a current source output. The modulators are comprised of mixers which function as current controlled attenuators, but, at a higher current level than available from the D/A Converter outputs. Since a circuit of this type is inherently broadband and the spectrum of the sampled waveform is repeated at multiples of the sampling frequency, a low-pass filter (LPF) is used to recover the desired spectrum and suppress the aliased spectrums. The two-pole RC filter provides a 1 kHz cutoff frequency (-6 dB) with a 40 dB/decade roll-off above the 1 kHz intercept point. R_{X1} is used to establish the circuit gain and is variable to facilitate optimization of mixer driver range during the build and test phase.

5.4.4.2 On-Line and Off-Line Peripherals Interfaces - There will be three peripherals - all essentially used for off-line operations:

- Operator Console
- Modem Acoustic Coupler
- Dual Flexible Disk

The proposed operator console is a TI Silent 700 terminal. The interface is a standard RS232 serial data link operating at a rate of 300 bauds. The terminal provides an operator a means of controlling the simulator to run tests, store data, perform calibaration and exchange data over phone line with the processor used for program development . A hard copy terminal was chosen to provide the operator with a permanent record of similar commands and results. The RS232 port on the SBC 86/12 board is to be used for the operator console.

The Modem Acoustic Coupler is of the Answer/Orginate type. The interface is standard 300 baud RS-232 serial data link. Mark/Space frequencies in the answer/originate mode are Bell 103 standard 1270/1070 HZ and 2225/2025 HZ. Use of this modem provides the capability of loading the simulator disk from any offline processor having dial-up data communications capability. In the case that the simulator is located in close proximity (100 ft.) to the offline processor, the modem may be bypassed with the high speed RS232 data link port on the processor.

The dual flexible disk interfaces directly with an SBC 202 controller which is comprised of a two card set. The controller transfers blocks of data between memory and disk and is set up by software. Data file format will be determined during the detailed design. Storage capacity is one-half megabyte per disk. Normally the second disk drive is used only to copy a data base for back-up purposes. The method of transporting a data base from offline processor to simulators would be over phone lines or by making a copy of a disk on a simulator and carrying or mailing it to another simulator.

Operational programs will be provided to control the operator console, transfer of data blocks over phone lines, and storage and loading of data blocks from disks. These programs will be located in ROMS on the CPU board and start executing immediately upon power-up or front panel reset.

5.4.5 Organization of Data

Data is organized on a flexible disk as 77 tracks of 53 sectors of 128 bytes. In addition, the disk includes address marks and parity check bytes as overhead.

Data will be transmitted over phone lines in a similar, but not necessarily identical block structure. A parity check will be performed at the receiving location resulting in the retransmission of data containing errors.

Header information will be required such that variable or incomplete block length messages can be sent. Pointers are to be included to aid in the eventual reconstruction of data blocks into a contiguous area of memory to facilitate rapid DMA transfers.

5.4.6 On-Line Software Requirements

A minimum number of on-line programs will be resident in the simulator to perform critical real-time functions. These programs will be ROM-based and written in Assembly language using a maximum of 16K bytes of available memory. On-line programs are identified as the following:

- Initialization
- Console Handler
- Communications Handler
- Disk Handler
- Simulator Experiment Run
- Calibration - Modulator Gain Set*
- Self-Test
    - ROM Check-Sum
    - RAM read-after-write
    - Disk read-after-write

Upon power-up or front panel reset, the processor will initialize hardware and commence execution of the operator console handling program. This program will be a line oriented command interpreter with simple line editing capabilities. Typical commands include the ability to examine memory, modify memory, branch to new program, select timebase, store memory on disk and load memory from disk. Subroutines written for the console handler will be written to be used by other programs requiring operator interface.

The Disk handler program will be file oriented. A directory of current files will be maintained on the disk. Blocks of data on disk will be protected by parity and/or cyclic redundancy check. Capability will exist to allow the user to identify and recover from errors due to track imperfections on the disk. In addition, the user will be able to format a blank disk and copy a disk for back-up purposes.

The simulator experiment program will be a highly efficient, interrupt-driven Assembly language program that transfers blocks of data between memory and the D/A converters. When the memory list is exhausted, the program will automatically start over at the top of the list in the fashion an endless loop. The simulator experiment program may be terminated by the operator at any time.

Calibration routines will be provided to allow an operator to automatically set all modulators to maximum attenuation and to vary the attenuation on one modulator for adjustment of the mean power level at each tap. Verification data bases may be generated offline for a similar purpose. Self-test routines such as ROM checksum, RAM read-after-write, and Disk read-after-write will also be provided.

The communications program allows block data transfer interactively with a similar program in another processor. Block size should be 128 bytes, the block size of the flexible disk, and should be protected by parity and/or cyclic redundancy checks. Retransmission of message blocks will occur if errors are detected.

Capability is needed to accomodate messages of variable block length. There will be convenient procedures for recovery from losing the communications channel without retransmitting the entire message. Program execution should be fast enough to operate at 9600 baud as well as 300 baud.

* Not required for Flat Fading Simulator

5.5 DIGITAL CONTROLLER GROWTH PLAN

In the flat fading implementation, a minimal digital controller configuration will consist of the following items:

- SBC 86/12 CPU
- SBC 116 ROM/Serial I/O
- SBC 202 Disk Controller
- Single SBC 064 64K RAM
- Single DAC Card containing 8 DAC's
- Silent 700 Terminal
- Dual Flexible Disk
- Modem Acoustic Coupler
- ICS 80 12-Slot Chassis
- Firmware modules to control:
  - Terminal
  - Disk
  - Modem
  - Simulation

Immediate expansion to 256K bytes of RAM by adding SBC 064 cards is at the discretion of the Defense Nuclear Agency.

Up to four D/A converter cards (32 D/A's) can be added to this chassis before expansion is required. At this point, two D/A converter cards will be replaced by a Bus Extender card terminated by a Bus Repeater card in the second chassis. Up to ten D/A converter cards can be located in the second chassis.

Firmware can also be upgraded at any time. A variety of interactive calibration and self test programs is recommended as is discussed in Paragraph 5.4.6. In addition, MULTIBUS - compatible peripheral cards are available (i.e. GPIB instrument controllers, bubble memory, hi-speed floating point, etc.) if needed.

5.6 SIMULATOR PERFORMANCE VALIDATION

During the construction and final checkout phases of the simulator development program, a number of performance validation functions are to be performed. A combination of inspection, analysis, test and demonstration will be used to verify performance. These procedures will be described in a test plan that must be developed early in the program.

While in the construction phase, subassembly gain and swept frequency response will be measured. The allocations for subassembly gain will be taken directly from Figures 13 and 14 for the flat and selective fading units respectively. Frequency response allocations to components are based on producing less than 0.9 dB peak to peak flatness variation across any DSCS channel bandwidth, including the effects of input and output down or upconverters, if supplied. (See Table 15).

Table 15. Simulator flatness allocations.

(85 MHZ BAND)

ITEM	P-P FLATNESS
C1X	0.1
C2X	0.1
A3	0.25
M1X	0.25
C3I	0.1
FL-1J	0.2
C4I	0.1
A-1	0.25
C-5I	0.1
TDL-1	0.15
CN-1	0.15
C7I	0.1
A-2	0.25
C-8I	0.1
M-2X	0.25
C-9X	0.1
FL-4X	0.2
C-10X	0.1
A-4	0.25
C-11	0.1
RSS =	0.775 dB

It will also be necessary to demonstrate that the simulator meets the interface criteria proposed in Tables 4 and 5. Other operational criteria to be verified are listed in the test matrix of Table 16.

An important parameter is the ability of the simulator to produce Rayleigh fading. This will be verified by inserting a sine wave modulated signal and recording the detected output on a strip chart recorder. A signal level versus time analysis of the resulting recording will be used to determine the percent of time the signal exceeds a set of quantized levels. This cumulative frequency distribution will be compared to that of a Rayleigh distribution. Mean fading rates, and the dynamic fading range will also be determined by inspection of these recordings.

Characteristics of components such as filters, amplifiers and D/A converters are verified by vendor data. Some of these units, at the discretion of General Electric, will be subject to an incoming performance verification. Passive elements, such as hybrids, couplers and isolators are purchased on an off-the-shelf basis and are subject only to inspection on a lot basis by the vendor.

Table 16. Test matrix.

Section 3 Paragraph Number and Title*		Insp	Anal	Test	Demo	Document
3.2.1.1.1	Flat Fading				X	
3.2.1.1.2	Freq. Selective Fading				X	
1.3.2.1.3	Amplitude & Phase Distributions		X			
3.2.1.1.4	Scattering Function		X			
3.2.1.2	Delay Line Characteristics		X			
3.2.1.3	Fading Rates to be Simulated				X	
3.2.1.4	Dynamic Fading Range				X	
3.2.1.5	Delay Line Power Distribution				X	
3.2.1.6	Tap Mean Power Setting			X		
3.2.1.7	Fading Signal Interference			X		
3.2.1.8	Resolution of D/A Converters		X			
3.2.1.9	Noise Figure		X			
3.2.1.10	Filter Requirements		X			
3.2.1.11	Frequency Accuracy Requirements		X			
3.2.1.12	Digital Controller	X				
3.2.1.12.1	Digital Controller Requirements		X			
3.2.1.13.1	Off-Line Software				X	X
3.2.1.13.2	On-Line Software				X	X

* Paragraph Numbers refer to those in the preliminary development specification.

Appendix A(*)

Appendix I(*)

EVALUATION OF $\frac{\gamma}{B}\, e^{(\gamma^4/2B^2)}\, K_{1/4}\, (\gamma^4/2B^2)$ (I.1)

$$\frac{\gamma}{B}\, e^{(\gamma^4/2B^2)}\, K_{1/4}\, (\gamma^4/2B^2) = \frac{2}{B^{1/2}}\, F\, (\gamma^2/B) \tag{I.2}$$

$$F(z) = \int_{-\infty}^{\infty} e^{(-x^4 - zx^2)}\, dx \tag{I.3}$$

$$F(z) = (\pi/2)^{1/2}\, z^{-1/2}\, \left(1 - \frac{0.191}{z^2} + \frac{0.197}{z^4} - \frac{0.112}{z^6}\right), \quad z \geq 1 \tag{I.4}$$

$$F(z) = 1.813 \exp\left(-0.675z + 0.271z^2 - 0.109z^3 + 0.031z^4\right), \quad -1 < z < 1 \tag{I.5}$$

$$F(z) = \frac{\pi^{1/2}\, e^{z^2}}{|z|^{1/2}}\, \left(1 + \frac{0.290}{z^2} - \frac{0.178}{z^4} + \frac{0.001}{z^6}\right), \quad z \leq -1 \tag{I.6}$$

The fit for F(z) is good to better than one percent.

(*) L.W. Wittwer, Unpublished Memorandum, "The Statistical Reconstruction of Scintillated Signals", April 1, 1979.

APPENDIX II MARGINAL DISTRIBUTIONS OF THE CHANNEL SCATTERING FUNCTION

The scattering function discussed in paragraphs 3.1 and 3.2 and illustrated in Figure 8 can be condensed into two marginal distributions for evaluation of critical delay line parameters.

Integration over the frequency variable f provides the delay power density distribution function

$$S(\tau) = \int_{-\infty}^{\infty} S(f, \tau)\, df \quad . \tag{II.1}$$

This is simply the mean power distribution along the delay line. Evaluation of $S(\tau)$ for the worst conditions expected resulted in the curve appearing in Figure 10. Parameter values used in $S(f, \tau)$ were

$f = 7.5$ MHz
$\tau_o = 1.0$ MS
$\sigma_\phi = 160.$
$f = 13.4$ MHz

Assuming 2 ns tap spacing, 95% of the power in $S(\tau)$ is distributed over only eighteen taps, six before and twelve after the peak in the marginal density curve. Also, 99% of the power appears by tap 26, and 99.9% by tap 38. For the given power distribution, a 50 tap line is clearly conservative design, but this number of taps will be maintained to provide additional testing flexibility for future experiments.

Integration over the delay variable τ yields the other marginal distribution, the frequency power density distribution function

$$S(f) = \int_{-\infty}^{\infty} S(f, \tau)\, d\tau \quad . \tag{II.2}$$

Using the same parameters as before, a plot of S(f) was made and is shown in Figure 1. Integration of S(f) then reveals the cutoff points containing a given fraction of the total power. This may be done analytically, since S(f) has a Gaussian characteristic

$$S(f) = Ke^{-(\tau_o \pi f)^2} . \qquad (II.3)$$

Thus, for 99.9% of the power

$$\frac{2}{\sqrt{\pi}} \int_0^{\tau_o \pi f} e^{-f^2} df = .999 \qquad (II.4)$$

and

$$f = .742/\tau_o \qquad (II.5)$$

This implies a Nyquist rate of about 1.5 τ_o^{-1}, hence the design sampling rate of 2 τ^{-1} for the worst case τ_o = 1 ms is a conservative choice.

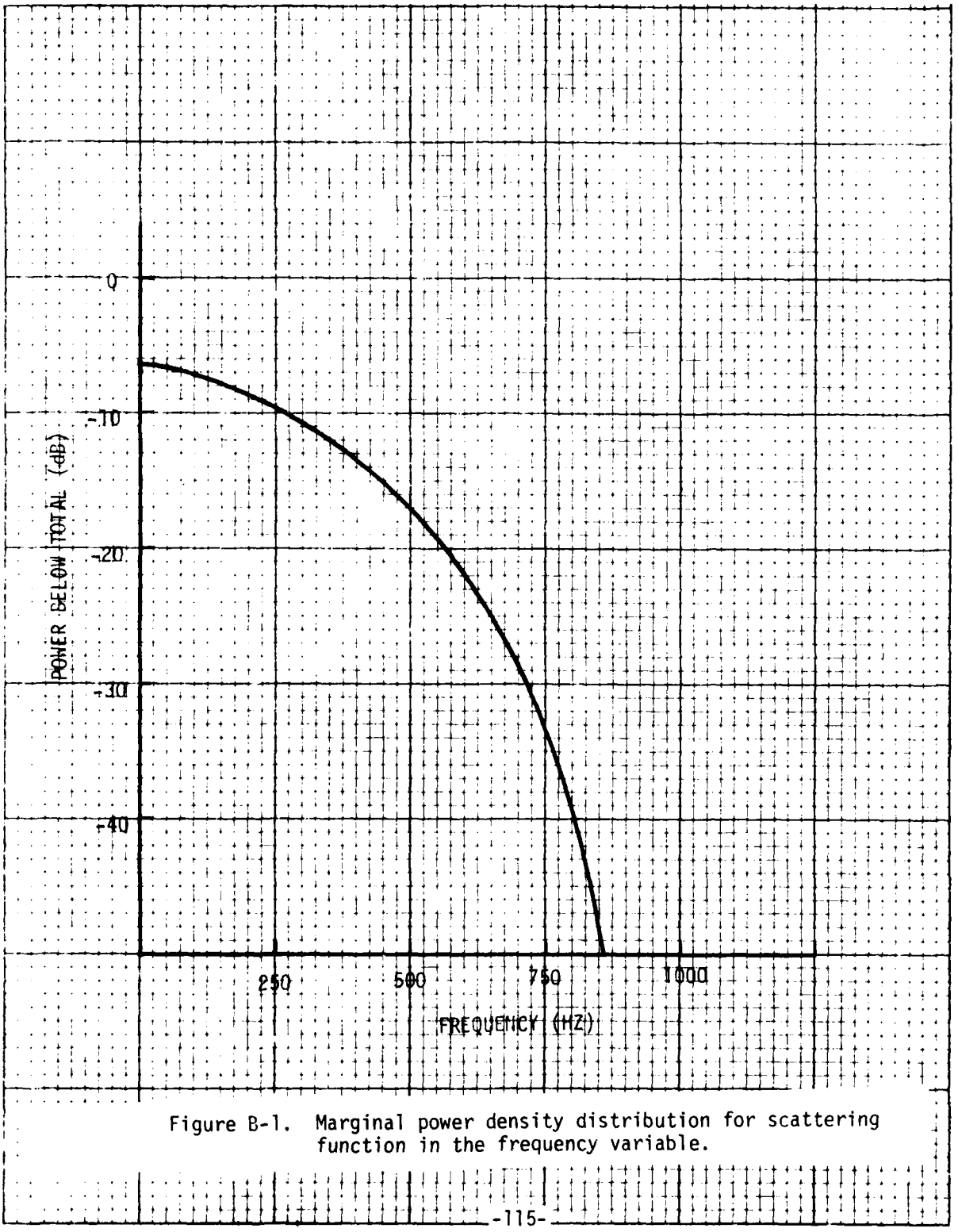


Figure B-1. Marginal power density distribution for scattering function in the frequency variable.

Appendix C

APPENDIX III DISTORTION AND INTERFERENCE IN DIGITALLY RECONSTRUCTED SIGNALS

The digital signal processing techniques used in reconstruction of the fading envelope will create a certain amount of signal distortion and interference. A very fast sampling rate (D/A data rate) will minimize the problem, but a fast sampling rate also strains the capabilities of the central processor in terms of speed and memory. A compromise between minimum distortion and interference may be found.

If the original analog fading waveform $x_a(t)$ has a spectrum $X_a(\omega)$ then the output of a D/A converter which holds each sample $x_a(nt)$ for T seconds is

$$x_f(t) = \sum_{n=-\infty}^{\infty} x_a(nT)\, p(t-nT), \qquad \text{(III.1)}$$

with spectrum

$$X_f(\omega) = \left(\frac{\sin \omega T/2}{\omega T/2}\right) \sum_{n=-\infty}^{\infty} X_a(\omega - n\omega_0) \qquad \text{(III.2)}$$

In Equation (A3-1), p(t-nt) is a unit pulse such that

$$p(t-nT) = \begin{cases} 1 & nT \leq t < (n+1)\,T \\ 0 & \text{elsewhere} \end{cases} \qquad \text{(III.3)}$$

The desired fading signal is given by the n=0 term in(III.2) the other terms are interference. The desired signal $X_a(\omega)$ is distorted, however,by the $(\sin \omega T/2)/\omega T/2)$ function.

If $x_a(t)$ is limited in bandwidth to W radians, the distortion and interference can both be minimized by choosing the data rate $1/T$ so that

$$W \ll \frac{2\pi}{T} = \omega_o = K\tau_o^{-1} \tag{III.4}$$

In Appendix the Nyquist rate was shown to be about $1.5\tau_o^{-1}$, τ_o being the decorrelation time. By driving the D/A at $10.0\,\tau_o^{-1}$ samples/sec, the distortion will be less than one percent, and the power ratio between the power in the interfering spectrums and the power in the primary signal spectrum is found approximately as

$$P_I = \frac{\int_{\omega_s/2}^{3\omega_s/2} \left(\frac{\sin \omega T/2}{\omega T/2}\right)^2 \exp(-(\omega - \omega_o)^2 \tau_o^2/4)\, d\omega}{\int_0^{\omega_s/2} \left(\frac{\sin \omega T/2}{\omega T/2}\right)^2 \exp(-\omega^2 \tau_o^2/4)\, d\omega} \tag{III.5}$$

$$= .104,$$

where the approximation involves discarding the higher-order spectrum contributions which are all nearly zero.

The 10% sampling interference is considered tolerable, particularly because the low-frequency fading envelope signal components are responsible for most of the bad effects of fading. Note that the interference will nearly disappear for D/A data rates approaching the limit of 2 kilosamples/second. A fixed lowpass filter with a one kilohertz cutoff follows each D/A converter, hence the interference, which at multiples of the data rate is rejected. The filter thus allows reduction of the data rate to $2\tau_o^{-1}$ for small τ_o. Additional sin x/x type distortion will then be compensated by shaping the signal spectrum.

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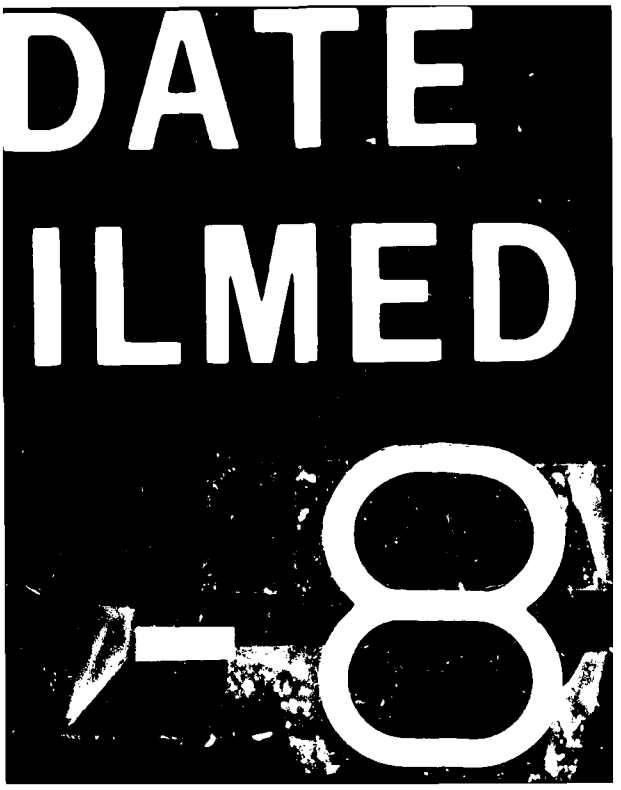
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